



Progress in Manufacture of Chips in South Korea

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Why is semiconductor so important ?

Security and military issues



Economical issues

연도별 반도체 수출 비중 단위: %



① 중앙일보

자료: 산업통상자원부

바이든 대통령, 반도체 대책회의 주요 발언

“미국이 21세기에도 세계를 이끌려면 반도체와 배터리 같은 첨단기술 분야에 공격적으로 투자할 필요가 있다.”

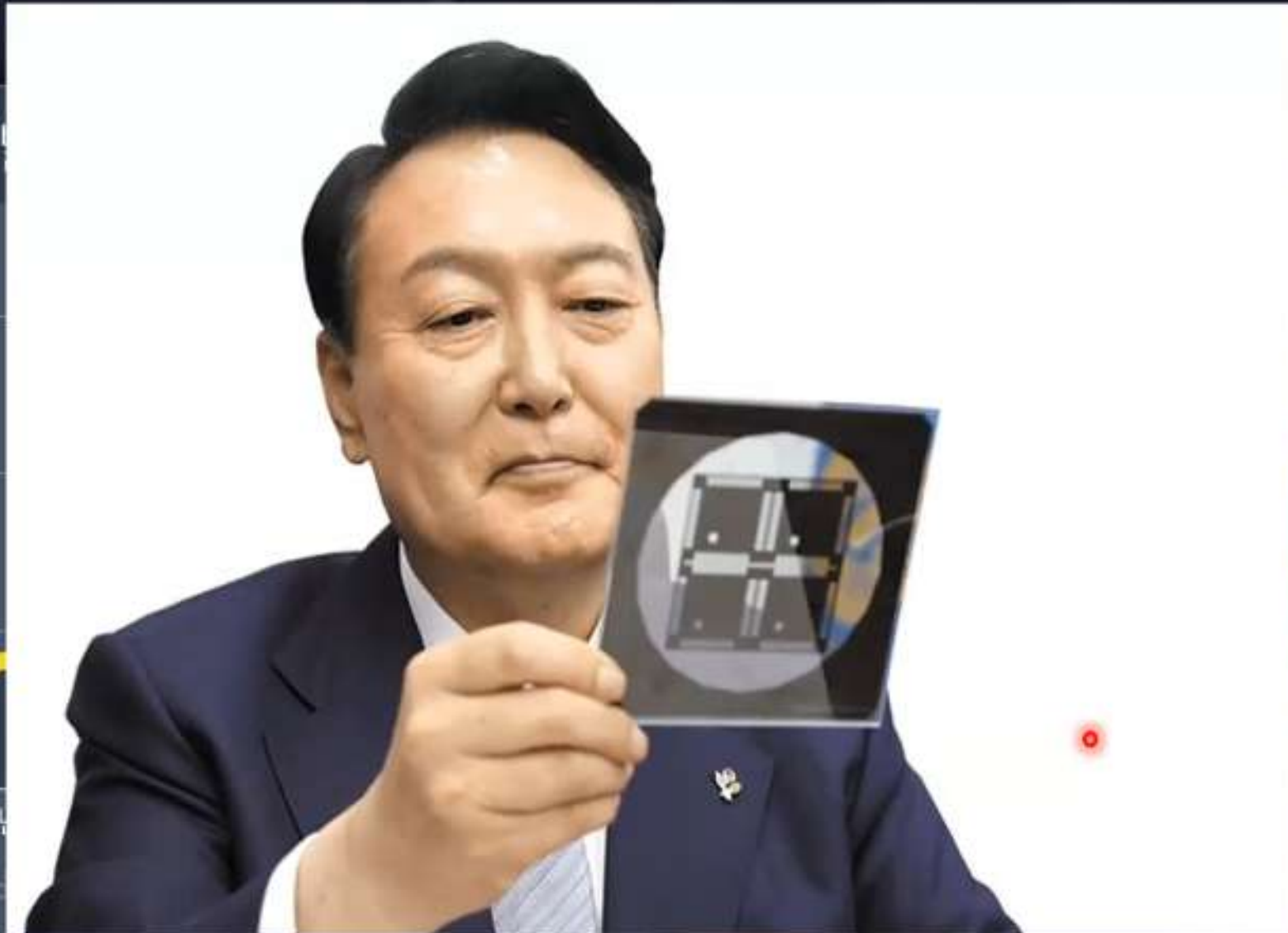
“과거의 인프라를 수리할 게 아니라, 반도체 칩, 웨이퍼와 배터리, 초고속 데이터 통신망 등 오늘날의 인프라를 새로 구축해야 한다.”

“중국은 반도체 공급망을 지배하려고 공격적으로 계획하고 있다. 중국과 세계는 기다려주지 않는다.”



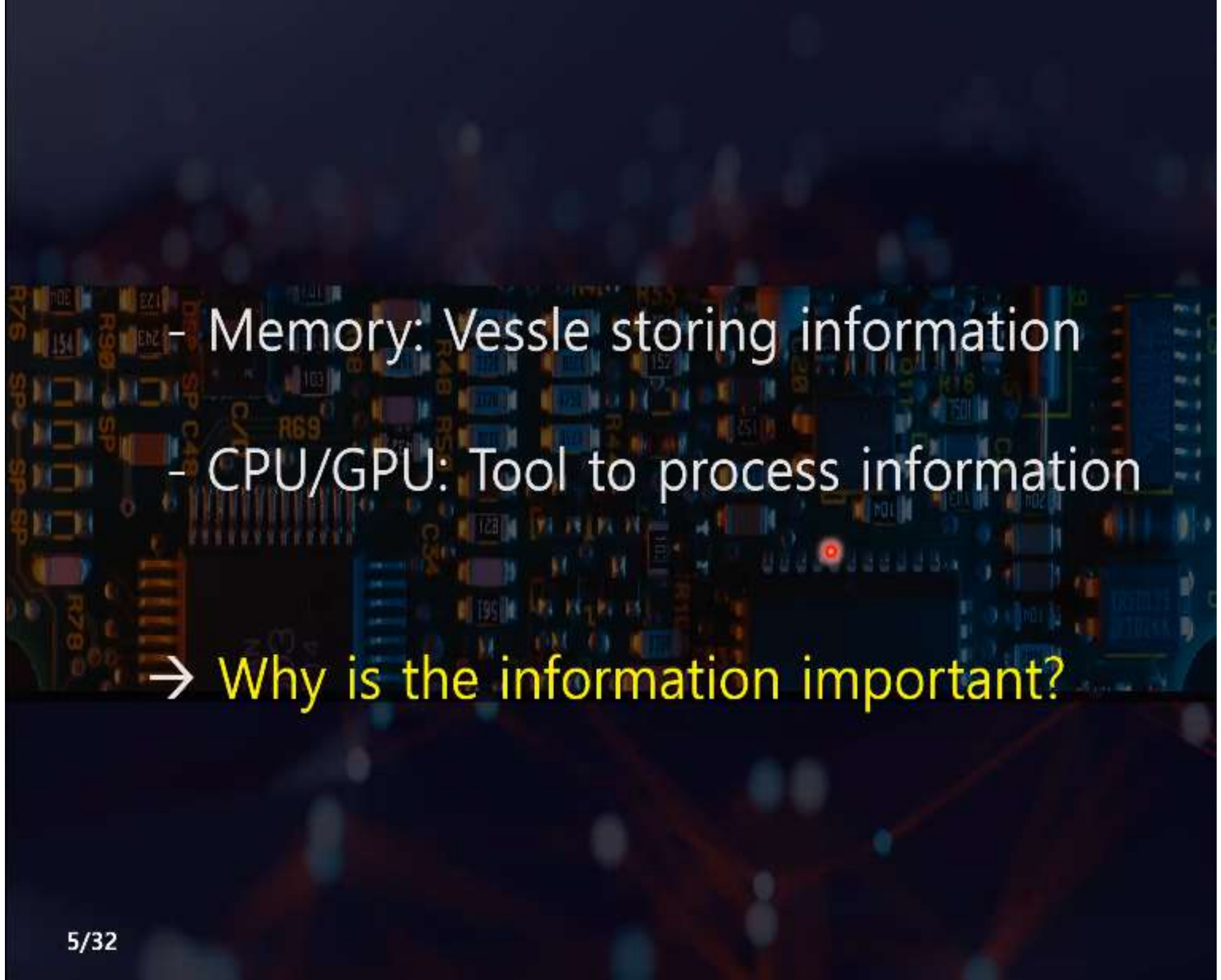
AP연합

Economical issues

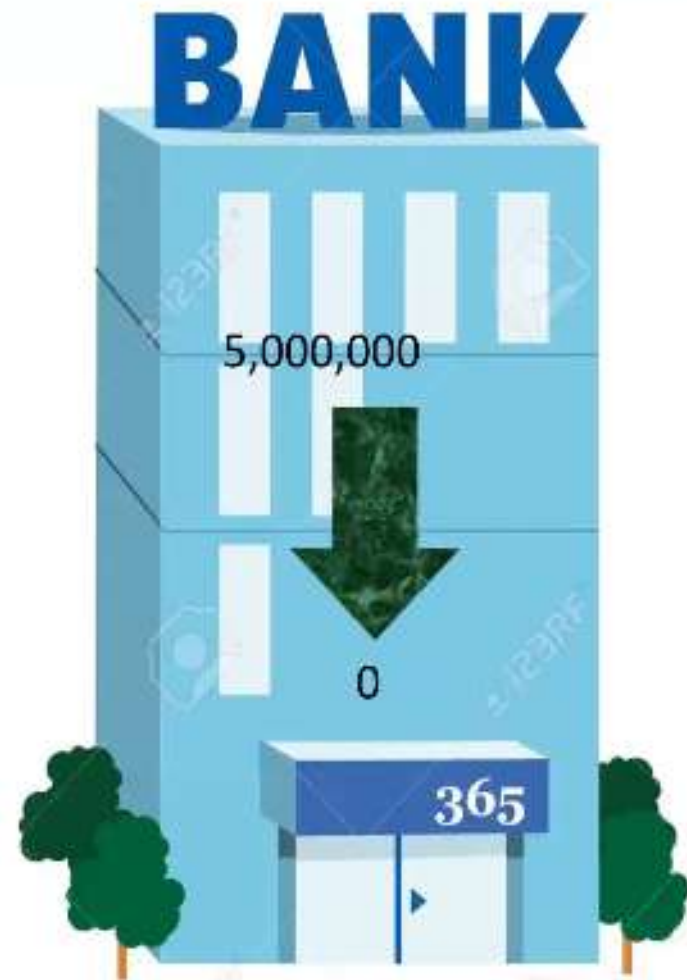


반도체
개발하려고
! 계획하고
과 세계는
! 않는다."

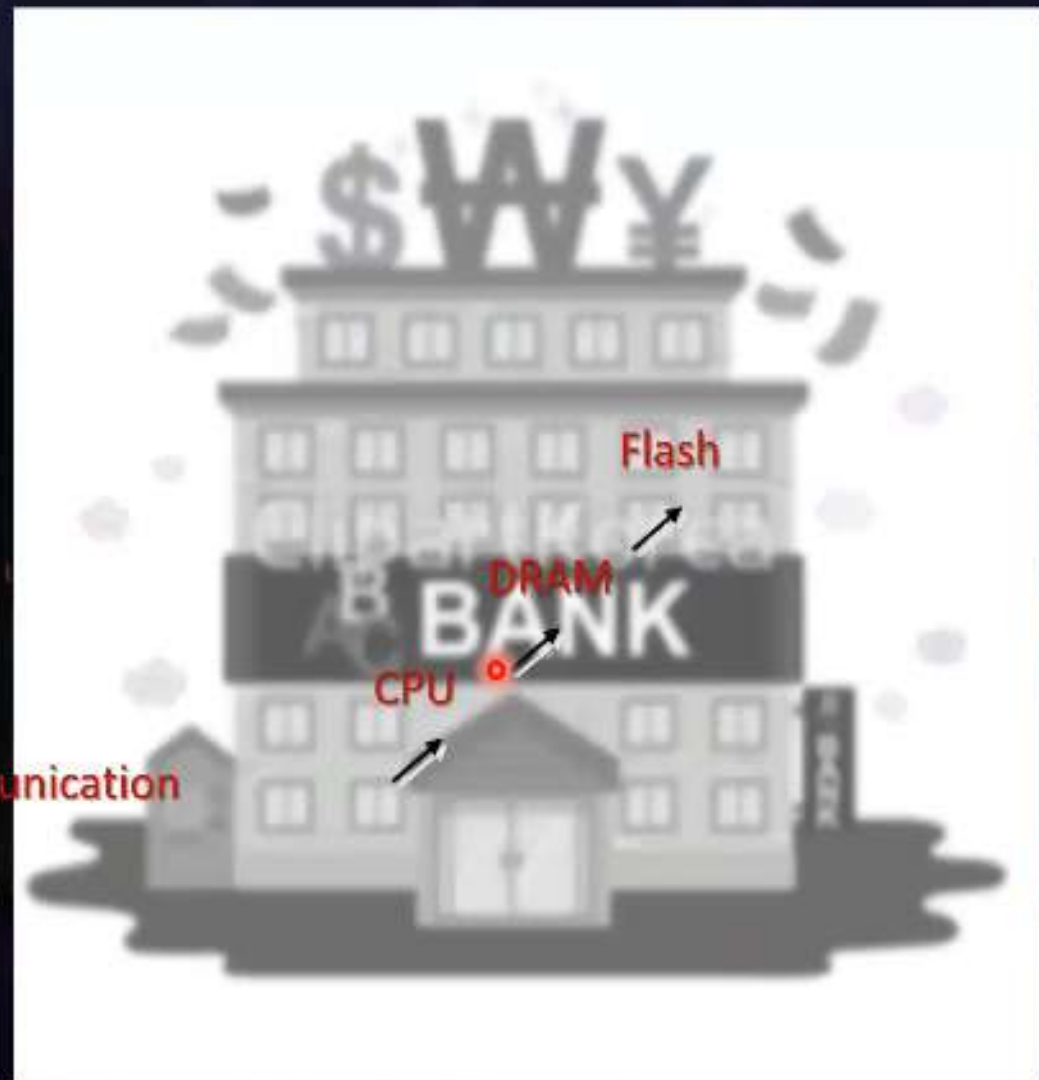
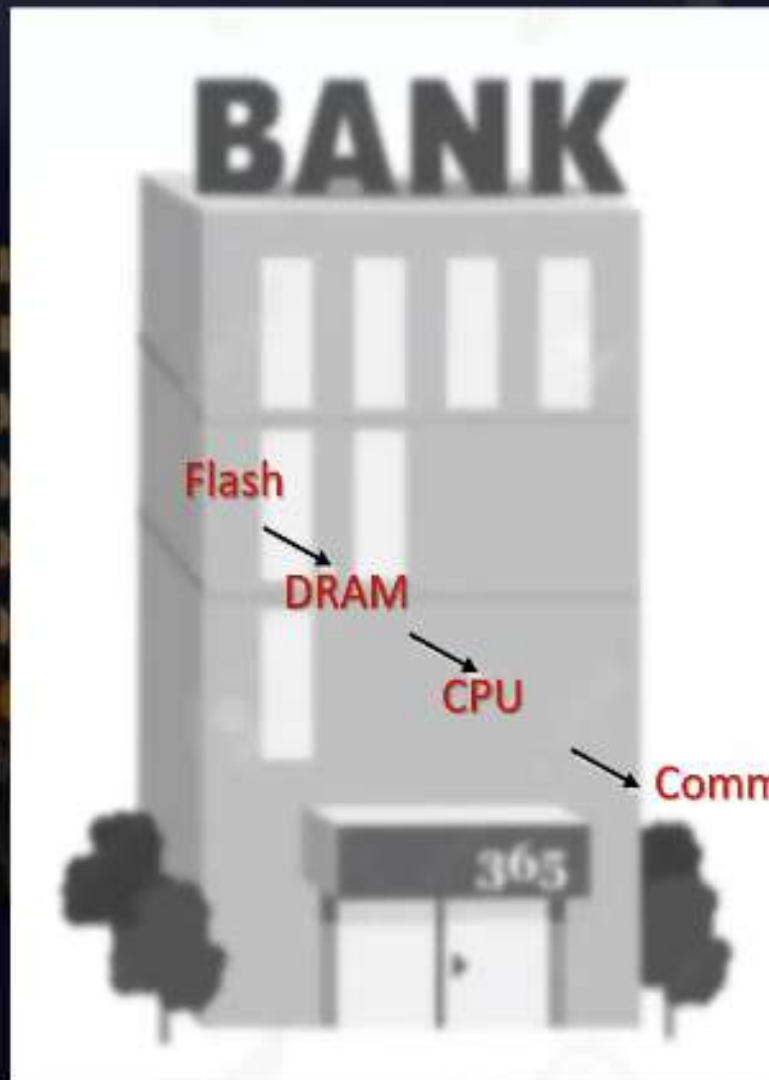
AP연합

- 
- Memory: Vessel storing information
 - CPU/GPU: Tool to process information
- Why is the information important?

Only information!



Only information!



Energy crisis

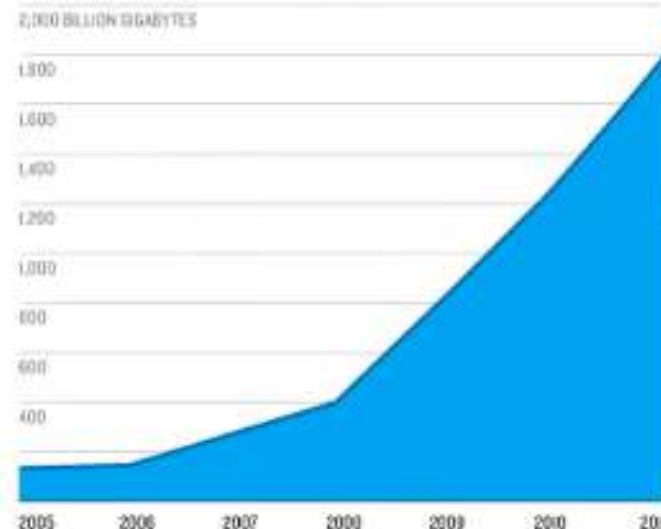
~44 zetabytes in 2020

10^{28} bytes

by 2040

Energy consumption of
U.S data centers in 2013
 $=3.3 \times 10^{17} \text{ J}$

Digital Information Created Each Year, Globally



2,000%

Expected increase in
global data by 2020

III

Megabytes

Video and photos stored
by Facebook, per user

75%

Percentage of all digital
data created by consumers

They gulp enough
electricity to power
all of NYC's households
for 2 years.



That's equivalent to the
output and pollution of

34
coal-fired
power plants.



(Annual output of a plant=450MW)
NRDC, Aug. 2014

Energy crisis

~44 zetabytes in 2020

By year 2040,

Total binary operation of

$$10^{40} \times 10^{-13} \text{ J}$$

per one binary operation

Total energy *consumption*

That's equivalent to the
output and pollution of

100billion
coal-fired
power plants.



Total energy *production*

$$>> 10^{25} \text{ J}$$

Building a House?

1. **Do everything by yourself:** design, buying materials, construction, etc.

→ Integrated Device Manufacturer (Intel (CPU) Samsung/SK Hynix (Memory))

2. **Let others do for you while you do what you can do best:**

I only design and hire others to make them. Or, I do not design but only fabricate what my customers have designed.

→ Fabless: Qualcomm, Nvidia, (Apple)

→ Foundry: TSMC, Samsung foundry, Intel foundry

Global Semiconductor Supply Chain

USA: Design / Software / Fabless

Japan: Material / Tools

Europe: Lithography / Material

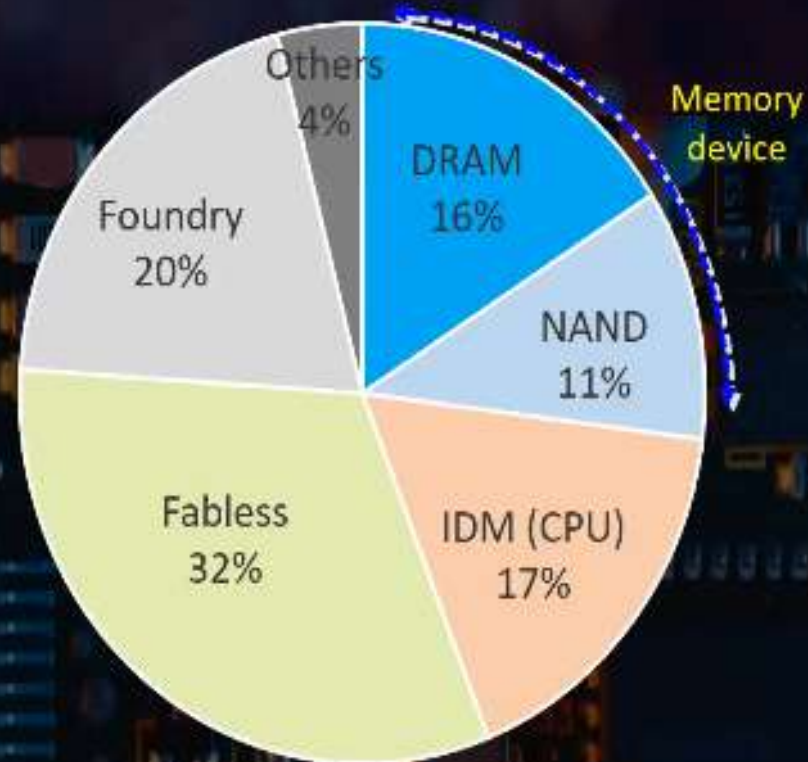
Taiwan: Foundry / Fabless → Double Si shield

Korea: Memory → Korea Semiconductor Security shield

China: Raw material / Fabless

**→ Chinese technology excavation (中國技術挖掘)
(Foundry/memory)**

Total semiconductor market share in 2020

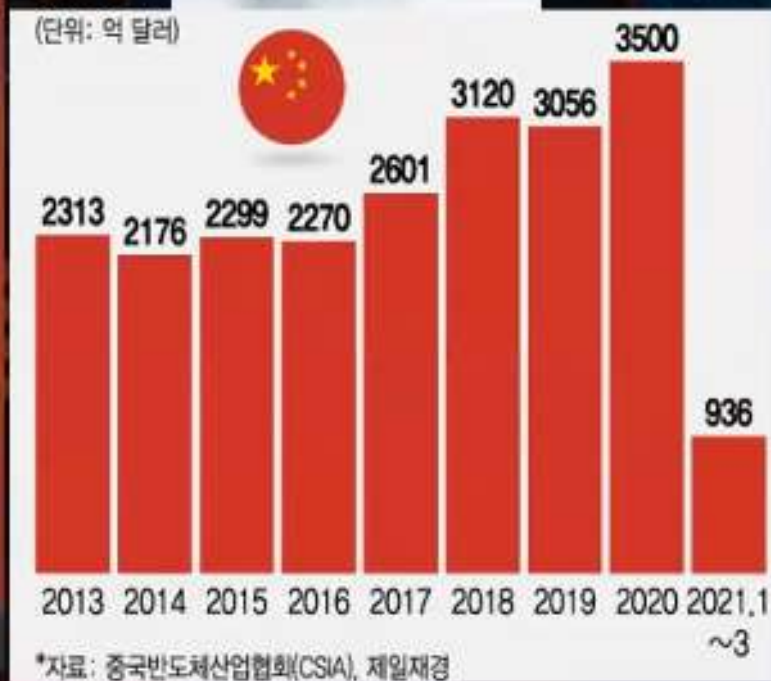


- **Memory 27%** (DRAM 16%, NAND 11%)
 - **IDM CPU** (Intel), **Fabless** (AMD, NVIDIA, Qualcomm)
 - **Foundry** (TSMC, Samsung, GlobalFoundries)
- } **High barriers to enter**

Chinese History Resolution (中國歷史決議)



Chinese History Resolution (中國歷史決議)





REPORT TO THE PRESIDENT Ensuring Long-Term U.S. Leadership in Semiconductors

Executive Office of the President
President's Council of Advisors on
Science and Technology

January 2017



The President's Council of Advisors on Science and Technology

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Scripps Institution of Oceanography

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President
Mundie & Associates

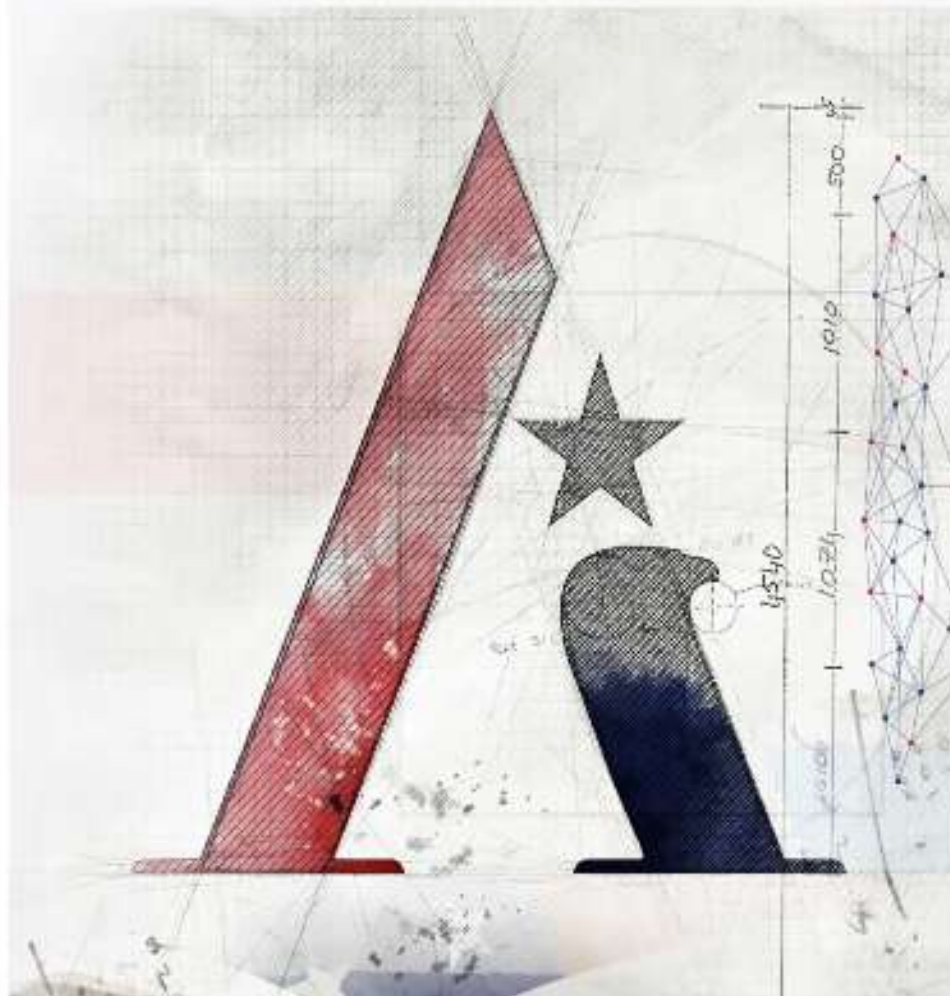
Staff

Ashley Predith
Executive Director

Jennifer L. Michael
Program Support Specialist

Final Report

National Security Commission on Artificial Intelligence



NATIONAL
SECURITY
COMMISSION
ON ARTIFICIAL
INTELLIGENCE

COMMISSION MEMBERS

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José-Marie Griffiths

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Andrew Moore

Final Report

National Security Commission on Artificial Intelligence



COMMISSION MEMBERS

p. 5: We do not want to overstate the precariousness of our position, but given that the vast majority of cutting-edge chips are produced at a single plant separated by just **110 miles of water from our principal strategic competitor**, we must reevaluate the meaning of supply chain resilience and security.

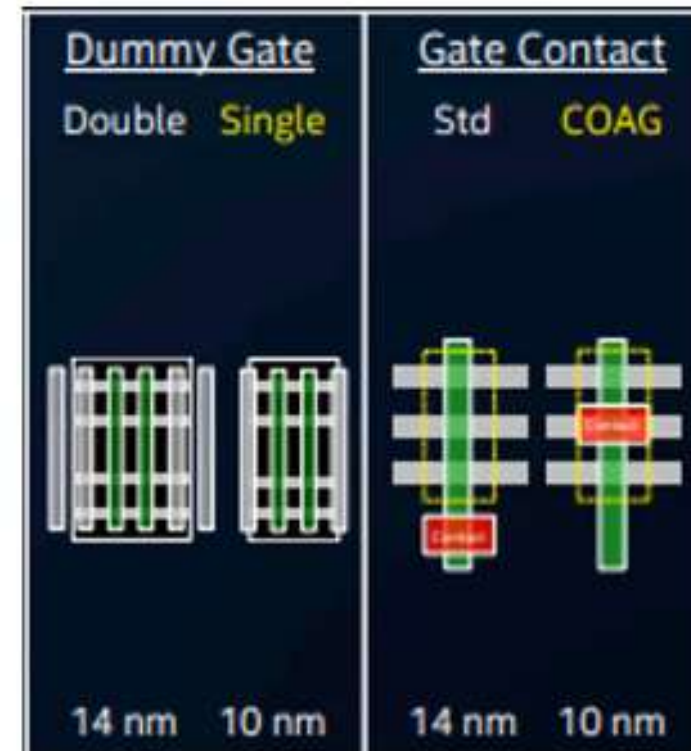
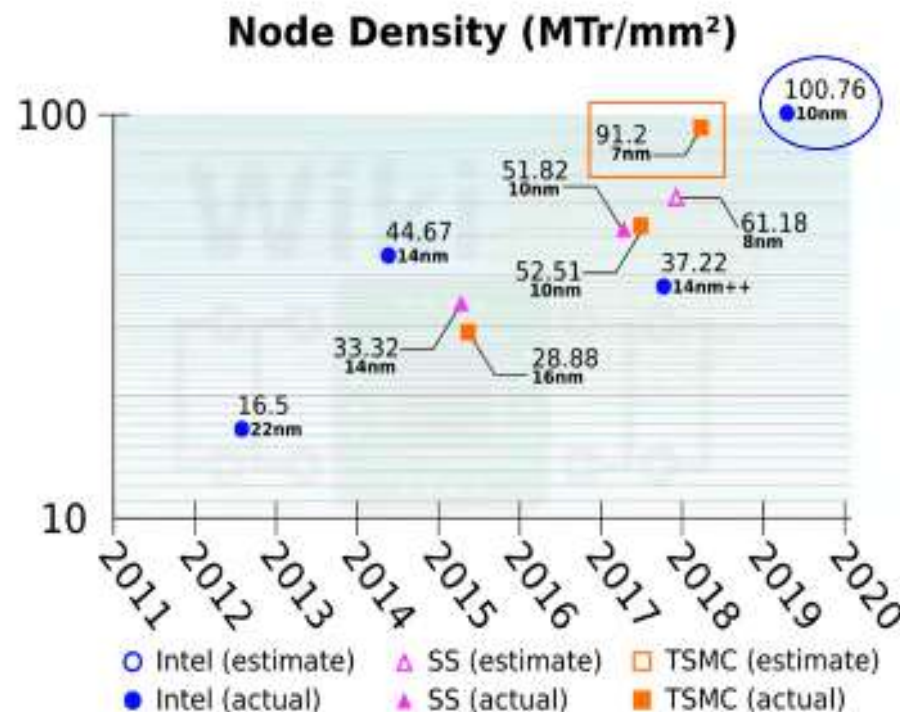
José-Marie Griffiths

Katharina McFarland

Andrew Moore

Intel 10 nm vs Qualcomm 7 nm (TSMC)

- Intel: Reduced chip size by hyper scaling



- By adopting Hyper Scaling (Single Dummy Gate, COAG (contact over active gate)), Intel 10 nm process accomplished higher transistor density than TSMC 7 nm process.

Intel 10 nm Where does Qualcomm's next CEO fit into the ongoing evolution of the chipmaker? (AC)

➤ Intel: Reduce



○ Intel (estimated)
● Intel (actual)

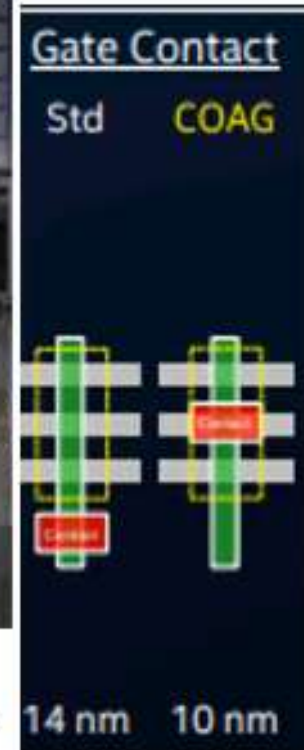


Qualcomm's new CEO Cristiano Amon poses for photos in the lobby at Qualcomm headquarters in San Diego. (Eduardo Contreras/The San Diego Union-Tribune)

Amon is a proponent of "coopetition," where rivals collaborate on certain things while competing in others. When Intel Chief Executive Pat Gelsinger recently laid out plans for the semiconductor giant to begin manufacturing chips for outside companies at its factories, Qualcomm signed on in support.

- By adopting H Intel 10 nm pro

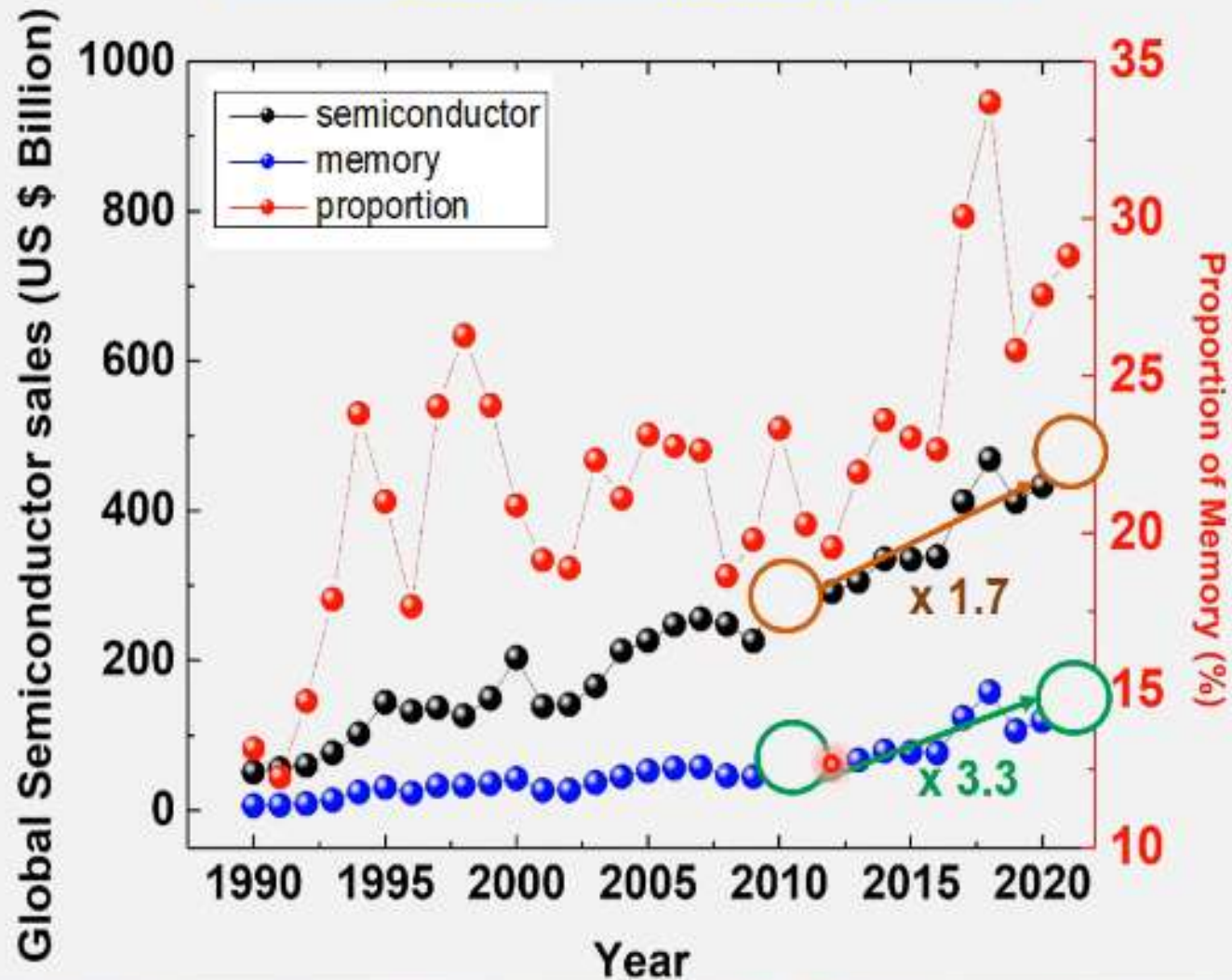
"Like me, Cristiano recognizes the need for a more balanced supply chain and advanced manufacturing operations in the U.S. and Europe to provide geographically diverse capacity at scale for their products," said Gelsinger in an email response to questions. "We are excited to develop a closer relationship with Qualcomm."



active gate)),
3 7 nm process.

Past

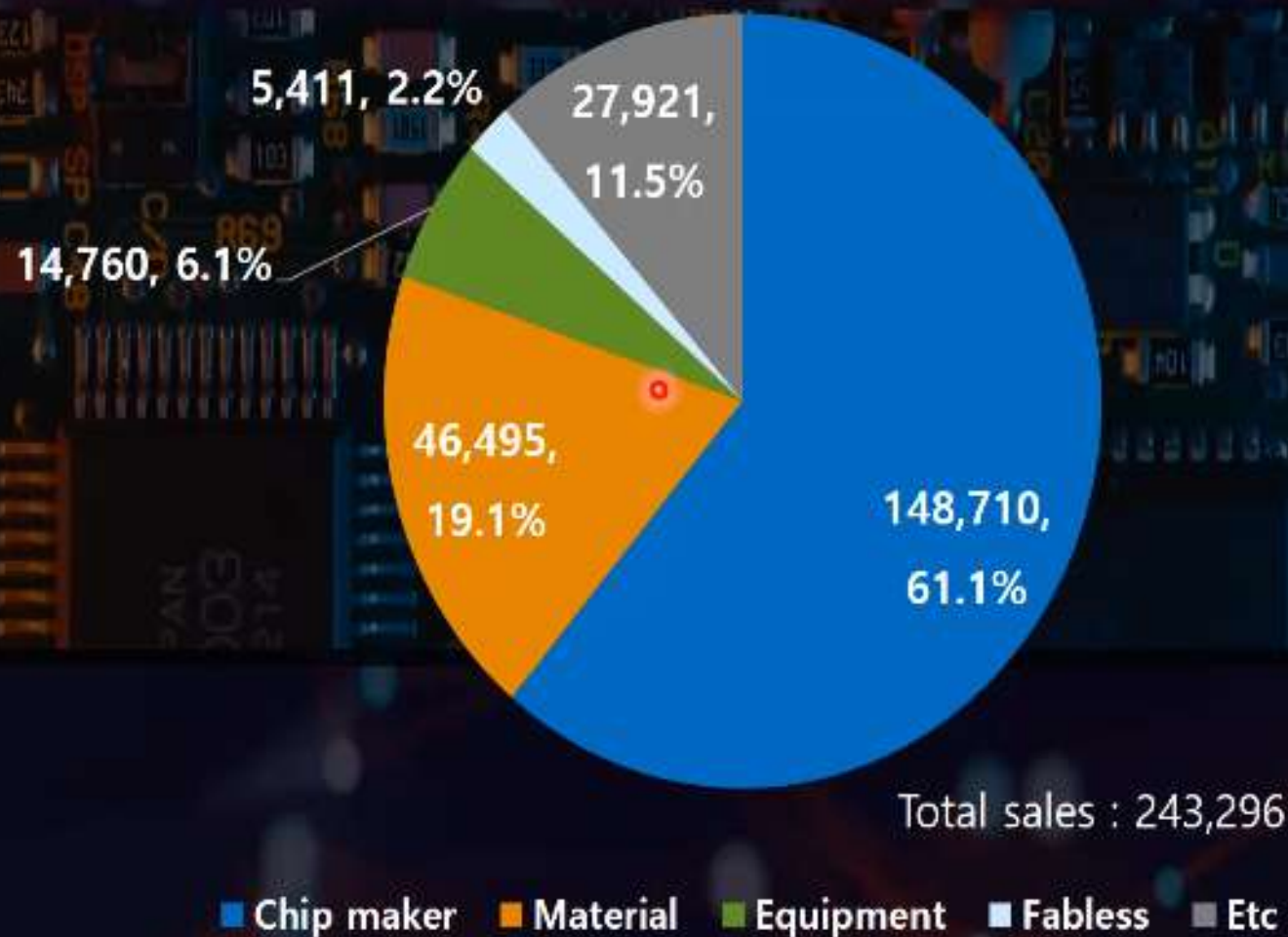
From 2011 to 2021
Semiconductor : 300 → 500 Billion \$
Memory : 45 → 150 Billion \$



Present

Semiconductor industry sales and share in 2021

(Unit : million \$, %)



Future



From 2020 to 2030
Semiconductor : 446 → 1351 B \$ (3 times)
Memory : 133 → 467 B \$ (3.5 times)

Source: SEMI

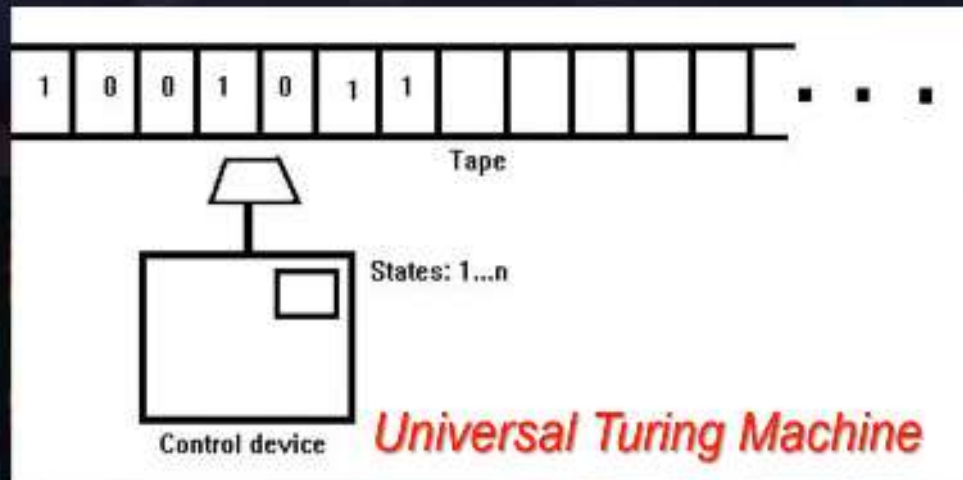
ON COMPUTABLE NUMBERS, WITH AN APPLICATION TO
THE ENTSCHEIDUNGSPROBLEM

By A. M. TURING.

[Received 28 May, 1936.—Read 12 November, 1936.]

The “computable” numbers may be described briefly as the real numbers whose expressions as a decimal are calculable by finite means. Although the subject of this paper is ostensibly the computable *numbers*,

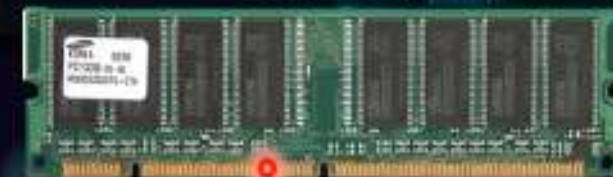
How does a computer work ?



Storage



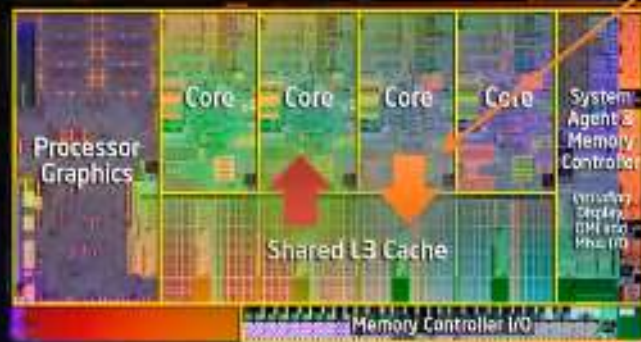
Memory



DRAM

CPU + cache

Fastest



CPU

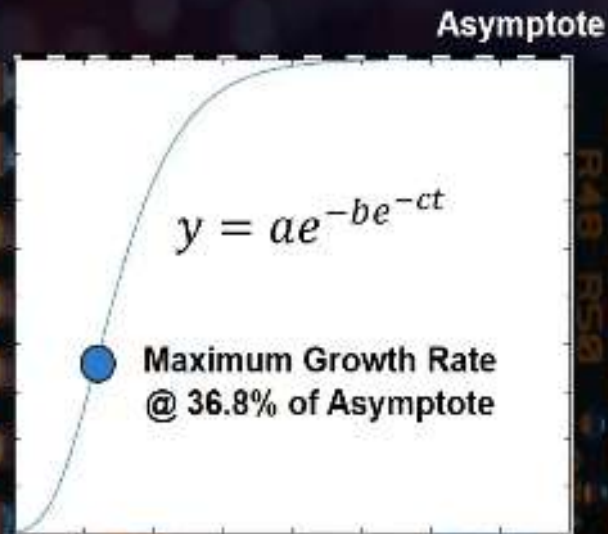
(Intel Sandy Bridge 2011)

SRAM (for cache)

Very fast

Why memory?

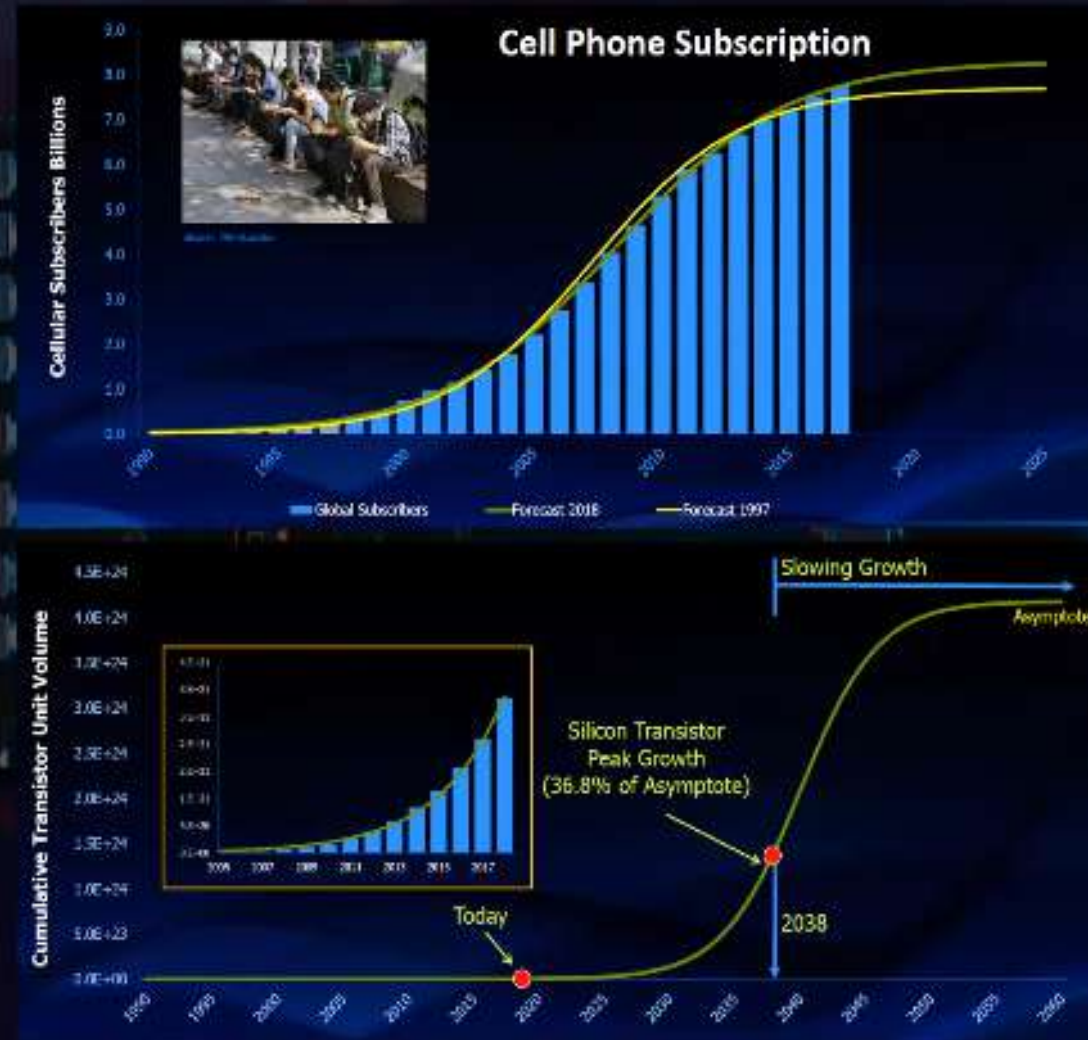
“The Gompertz Curve”



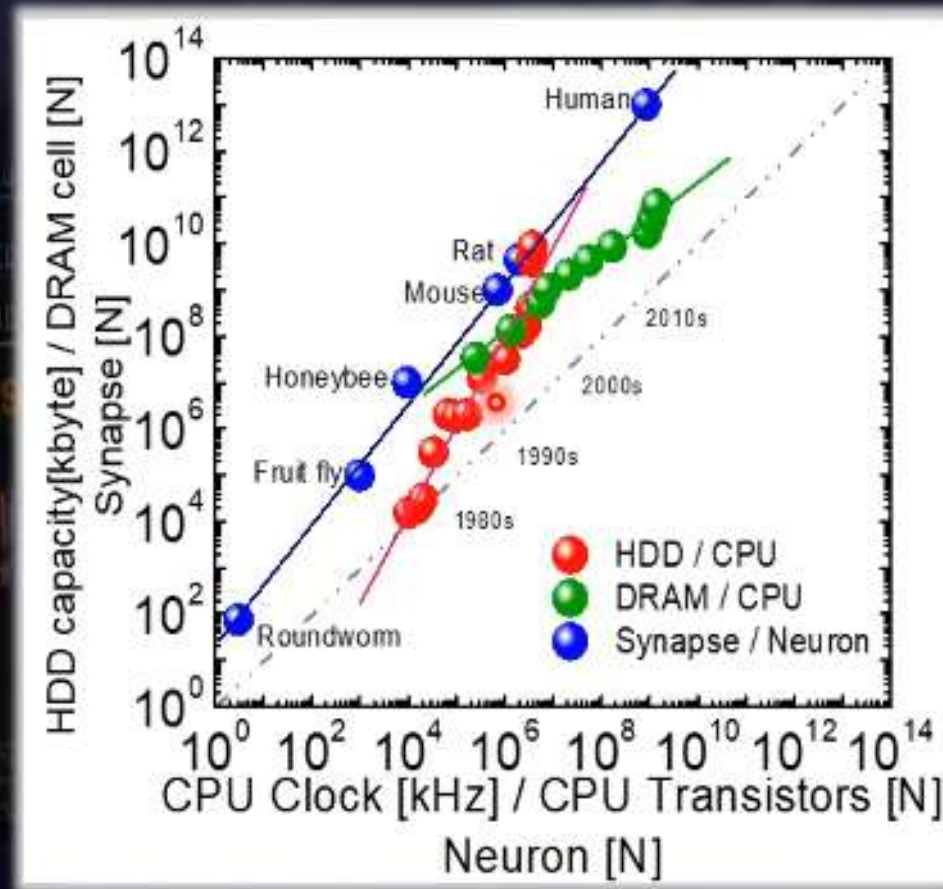
- Mathematical model for time series

➤ 99.9 % of
Transistors are in
memory!

❖ Prediction by Gompertz Forecast



Computer (find answer) vs. Brain (find best)

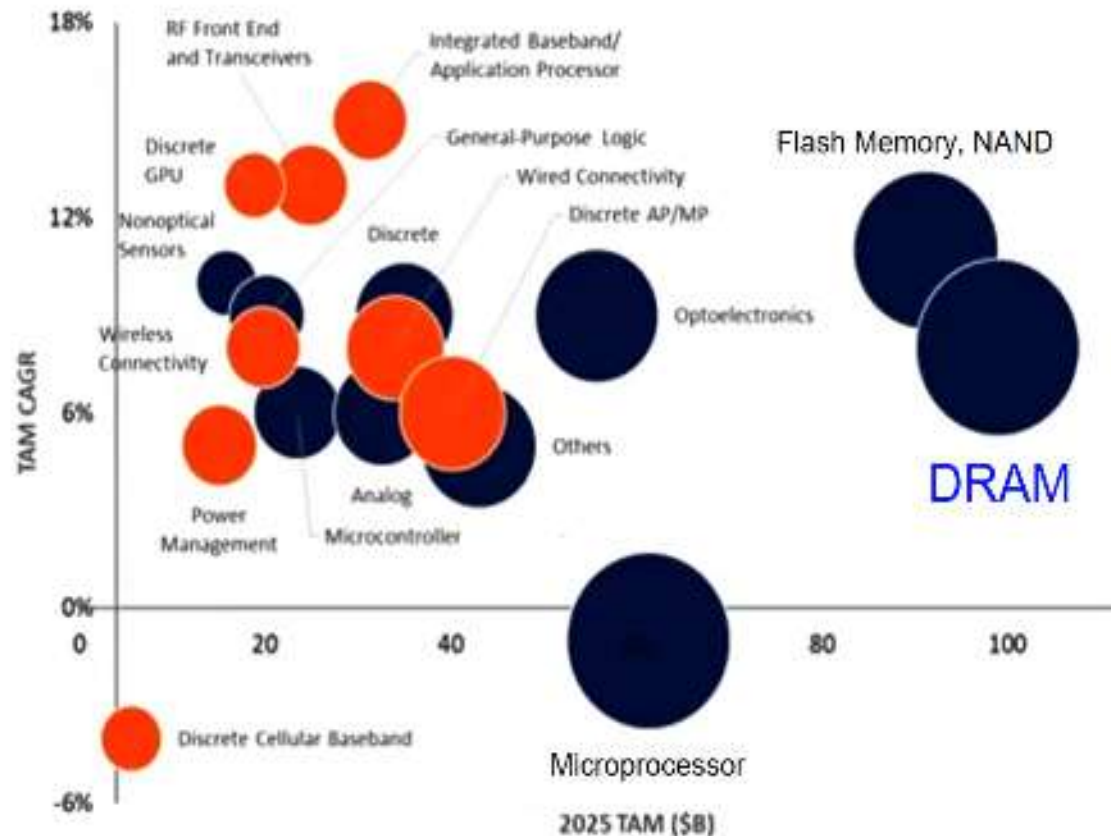


1987 → 2019
CPU clock : ~ 1000 times
Memory : ~ 100,000 times

Synapse/Neuron ~ 10,000
TR in DRAM/CPU ~ 10 - 100

Chip market prospect (up to 2025)

※ Semiconductor Revenue Forecast by Device Type Through 2025 (from Gartner)



Product	Market size	G/R
DRAM	\$100 billion	> 6%
NAND	\$90 billion	~10%
Microprocessors	\$60 billion	Decaying

* TAM(Total Addressable Market) :
CAGR(Compound Annual Growth Rate)

Business strategies of Semiconductor companies

➤ IDM, Fabless and Foundry: Dedicate to what they can do best

 Dedicates to CPU, Sell out flash business to SK Hynix (@20. 11), Extend to Foundry

 Try to merge Arm (@20. 9). Dedicates to what they can do well.

 Invest 100B USD\$ for next three years for foundry (@21. 4);
do not compete with customers !

 Co-invest Memory, Foundry and system LSI:
120 B USD\$ for next three years for memory and fo
but they have to compete with customers!

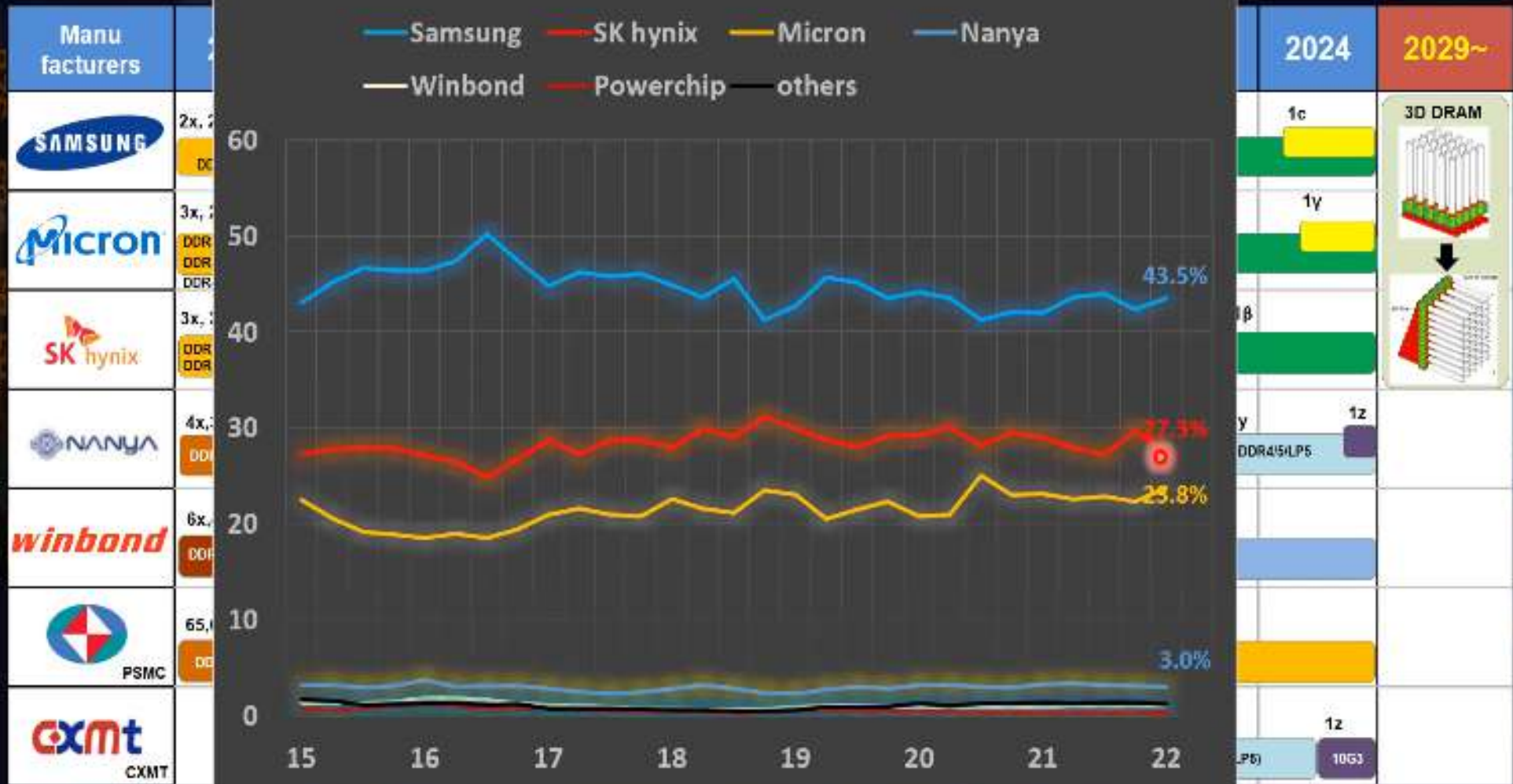
 Dedicated to Memory. Acquire Intel's Flash →
Solidigm
100 B USD\$ to build Yongin Semiconductor cluster



Global memory company: DRAM Roadmap

Manu facturers	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2029~
SAMSUNG	2x, 2y (nm) DDR3/LP3 DDR4/LP3/LP4/LPX/GDDR5/GBM2		1x DDR4/LP4X/GDDR6	1y DDR4/LPDDR4/ 4X/LP5/HBM3/GDDR6X		1z DDR5/LPDDR5X/GDDR7		1a DDR5/LPDDR5X/ iGDDR7X	1b	1c	3D DRAM 
Micron	3x, 2x, 2y (nm) DDR3/DDR4/LP3/HMC1/HMC2/1S DDR3/DDR4/LP3/LP4 DDR4/LPiGDDR5/GDDR6X/GDDR6		1x, 1xs DDR4/LPDDR4/GDDR6X	1y DDR4/LPDDR4	1z DDR4/DDR5/LPDDR5		1α DDR6/LPDDR6		1β	1γ	
SK hynix	3x, 2x (nm) DDR3/ DDR4/LP4/HBM1	2y, 2z DDR4/LP4/LP4X/GDDR5/HBM2		1x DDR4/LP4/LP4X iHBM2E/GDDR6	1y DDR4/DDR6/LPDDR4 iLPDDR5SX/GDDR6X		1z DDR5/LPDDR5 LPDDR5X	1α DDR6/LPDDR6X/GDDR7X		1β	
NANYA	4x, 3x (nm) DDR3/DDR4/LP3/LP4			2x DDR3/LP3/LP4			1x DDR4/DDR5/LP4		1y DDR4/5/LP5		1z
winbond	6x, 4x (nm) DDR2/DDR3/LP1/LP2		3x DDR3/LP3			25 nm DDR3/DDR4/LP3/LP4/LP4X, Auto			1x DDR4/LP4		
PSMC	65, 60, 40, 30 (nm) DDR/DDR2/DDR3/LPDDR2/LPDDR3							20 nm DDR3/DDR4			
CXMT					22 nm DDR4		1x 10G1 (DDR4/LPDDR4/4X)	1y 10G2 (DDR5, LP5)			1z 10G3

Global memory company: DRAM Roadmap



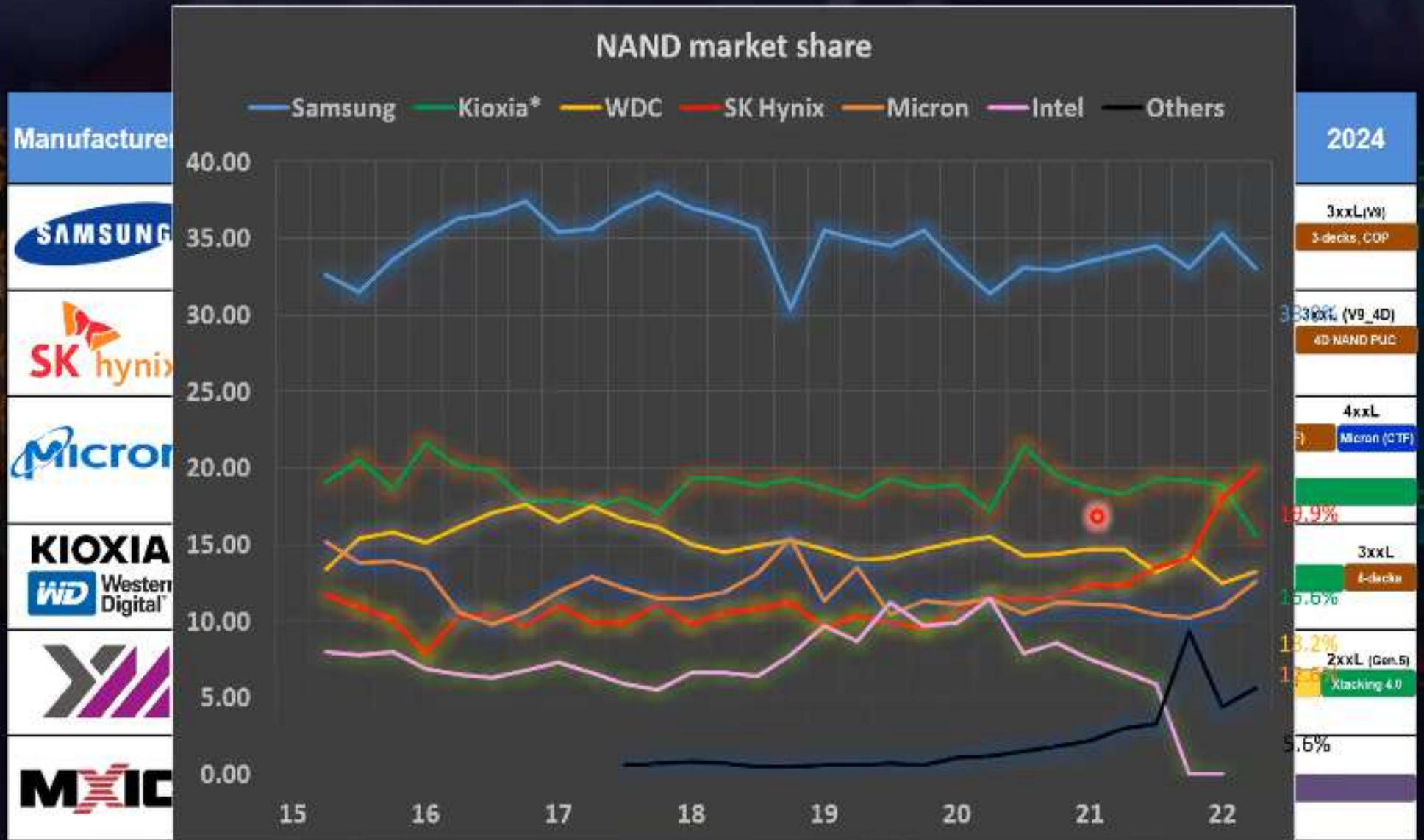
Memory Technology 2021 and Beyond – NAND, DRAM, Emerging and Embedded Memory Technology Trends, Techinsights

Global memory company: NAND Roadmap

Manufacturers	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
SAMSUNG	32L (v2) 20nm	48L (v3) 20nm	64L (v4) 20nm, 64GB TLC/QLC 256/512G TLC/H1T QLC	92L (v5) 20nm, 96Lx1 TLC/QLC 256/512G TLC/H1T QLC	128L (v6) 20nm, 64Lx2 256G/512G/1T	176L (v7) 2-decks, COP 512G/1T	2xxL (v8) 2-decks, COP	3xxL (v9) 3-decks, COP		
SK hynix	30 F-LiCS	36L (v2_3D) 31nm, 16GB MLC	48L (v3_3D) 31nm, 32GB TLC	72/76L (v4_3D) 31nm, 40L+32L 256G M8T/512G	96L (v5_4D) 20nm, 4d PUC, 48x2 512G/1T (TLC only)	128L (v6_4D) 14T, 4D PUC, 84x2 612G/1T (TLC only)	176L (v7_4D) 4D PUC, 88x2 512G/1T	238L (v8_4D) 4D NAND PUC	3xxL (v9_4D) 4D NAND PUC	
Micron	30 FG, CuA	32L 40nm, FG 384G TLC	64L 20nm, FG, 32Lx2 256G/512G TLC/H1T QLC 32L 128G TLC (eMMC)	96L 20nm, FG, 48Lx2 512G TLC/H1T QLC 32L 128G MLC (Low Temp.)	128L, 176L CTF Micron (CTF, 88x2) 144L Micron (CTF, 88x2) 612G TLC/H1T QLC	2xxL Micron (CTF) 1yyL Intel (FG), 3-deck, 48x3 512G TLC/H1T QLC	3xxL Micron (CTF) 2xxL Intel (FG)	4xxL Micron (CTF)		
KIOXIA WD Western Digital	3D UFS 19nm	24L (B1CS1) 19nm	48L (B1CS2) 19nm, 32GB TLC	64L (B1CS3) 19nm, TLC 128/256/512G TLC	96L (B1CS4) 19nm, 48Lx2 TLC/QLC 256/512G TLC/H1T Q	112L (B1CS6) 19nm, 2-decks, 123T 256/512G TH1T Q	160L (B1CS6) 2-decks, CuA, Split Gate	2xxL (B1CS7) 3-decks	3xxL 4-decks	
X			3D Xstacking	32L (Gen.1) Conventional MLC (64Gb)	64L (Gen.2) Xstacking, H-bonding MLC/TLC (256Gb)	128L (Gen.3) Xstacking 2.0, 64Lx2 TLC/512Gb/QLC (1.33Tb)	192L (Gen.4) Xstacking 3.0, 64Lx3	2xxL (Gen.5) Xstacking 4.0		
MXIC						48L (Gen.1) 3d NAND	96L (Gen.2) MLC/TLC 48Lx2			

Memory Technology 2020 and Beyond – NAND, DRAM, Emerging and Embedded Memory Technology Trends, TechInsights

Global memory company: NAND Roadmap



Memory Technology 2020 and Beyond – NAND, DRAM, Emerging and Embedded Memory Technology Trends, TechInsights

4D NAND Flash Memory

TLC NAND Process Technology Nodes

Company	Layer Count	Density (Gb/mm ²)	Decks	Planes	Shipping ⁽¹⁾
Micron	128	7.76	2	4	Yes
	176	10.27	2	4	Yes
	232	14.60	2	6	Yes
Samsung ⁽²⁾	128	6.91	1	4	Yes
	176	8.50	2	4	No
	>200	11.55	2	?	No
SK Hynix	128	8.10	2	4	Yes
	176	10.80	2	4	Yes
	238	14.39	2	4	No
Western Digital / Kioxia	112	7.70	2	4	Yes
	162	10.40	2	4	No
	212	?	2	?	No
YMTC	128	8.48	2	4	Yes
	232	15.20	2	6	Yes
Solidigm ⁽³⁾	144	12.86	3	4	Yes
	196	?	4	4	No

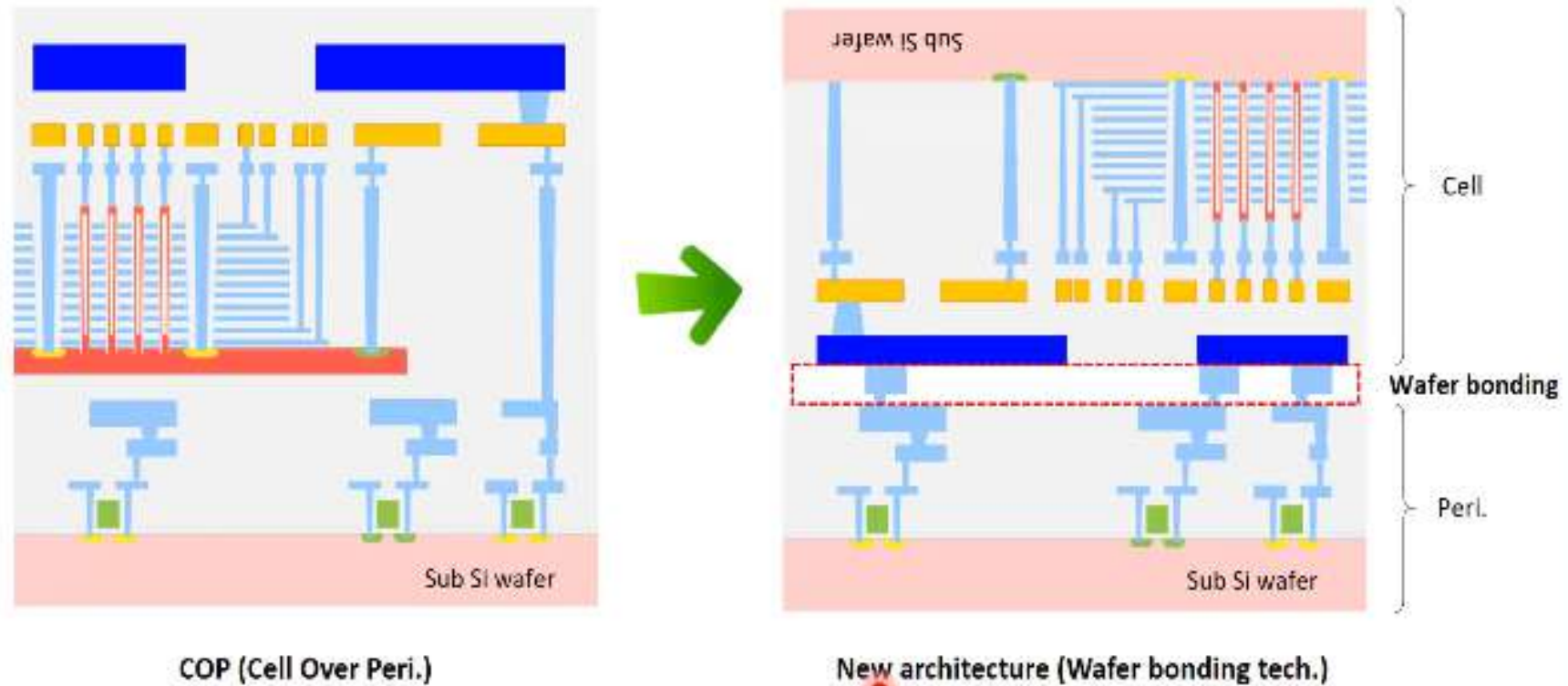
1. In SSDs currently available or sampling from 3rd party SSD/controller firms.

2. 176-layer and >200-layer density disclosed by Samsung at ISSCC.

3. Solidigm density is with QLC not TLC.

Next generation 4D NAND architecture

- Separation of Cell array & Peri. manufacture process using wafer bonding technology

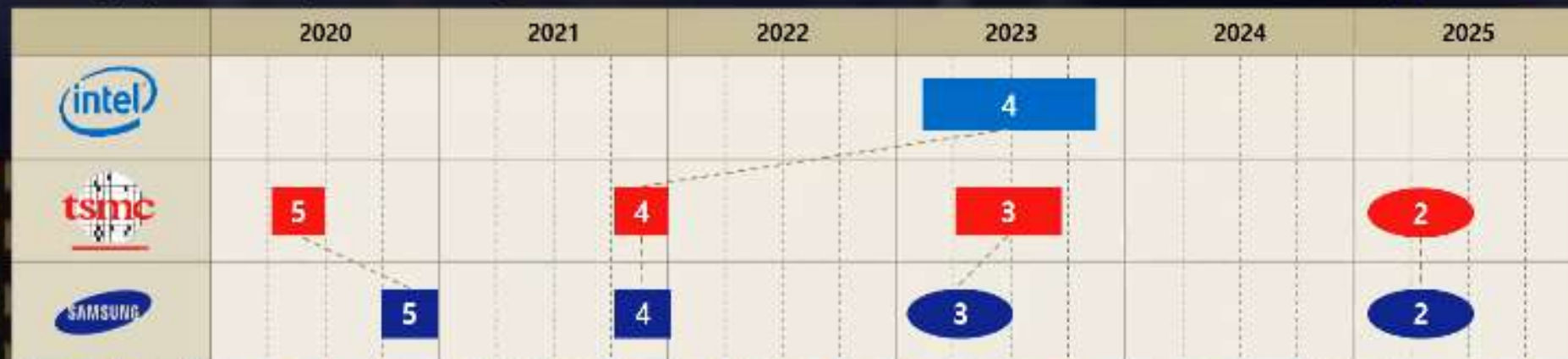


- Enable to use high temperature process (releasing heat budget limitation)
→ Improvement of cell characteristics (reliability and electrical performance)
- Reduce production period (parallel production of cell and peri. wafers)
- *Higher cost by increasing process steps*

Global Foundry Technology Roadmap

Logic process comparison (mass production)

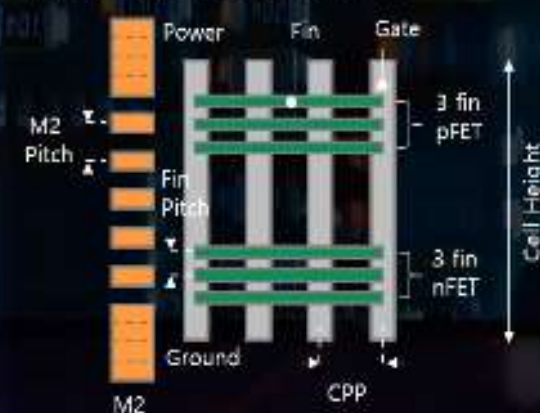
■ FinFET ● GAA



Main Logic process comparison

	Samsung	TSMC	Intel	Intel	Samsung	TSMC	TSMC
Node	5 nm		4 nm		3 nm		2 nm
Process Type	FinFET	FinFET	FinFET	FinFET	GAA	FinFET	GAA
CPP (nm) ⁽¹⁾	54	51	50	50	45	45	?
M2P (nm) ⁽²⁾	36	34	45	45	32	28	?
Tracks ⁽³⁾	9	9	5.33	9	9	9	?
CH (nm) ⁽⁴⁾	324	306	240	405	288	256	?
CPP x CH	17,496	15,606	12,000	20,250	12,960	11,340	?
Mass Product	Q4 2020	Q2 2022	2023		2023	Q2/Q3 2023	H2 2025

7.5 track logic cell



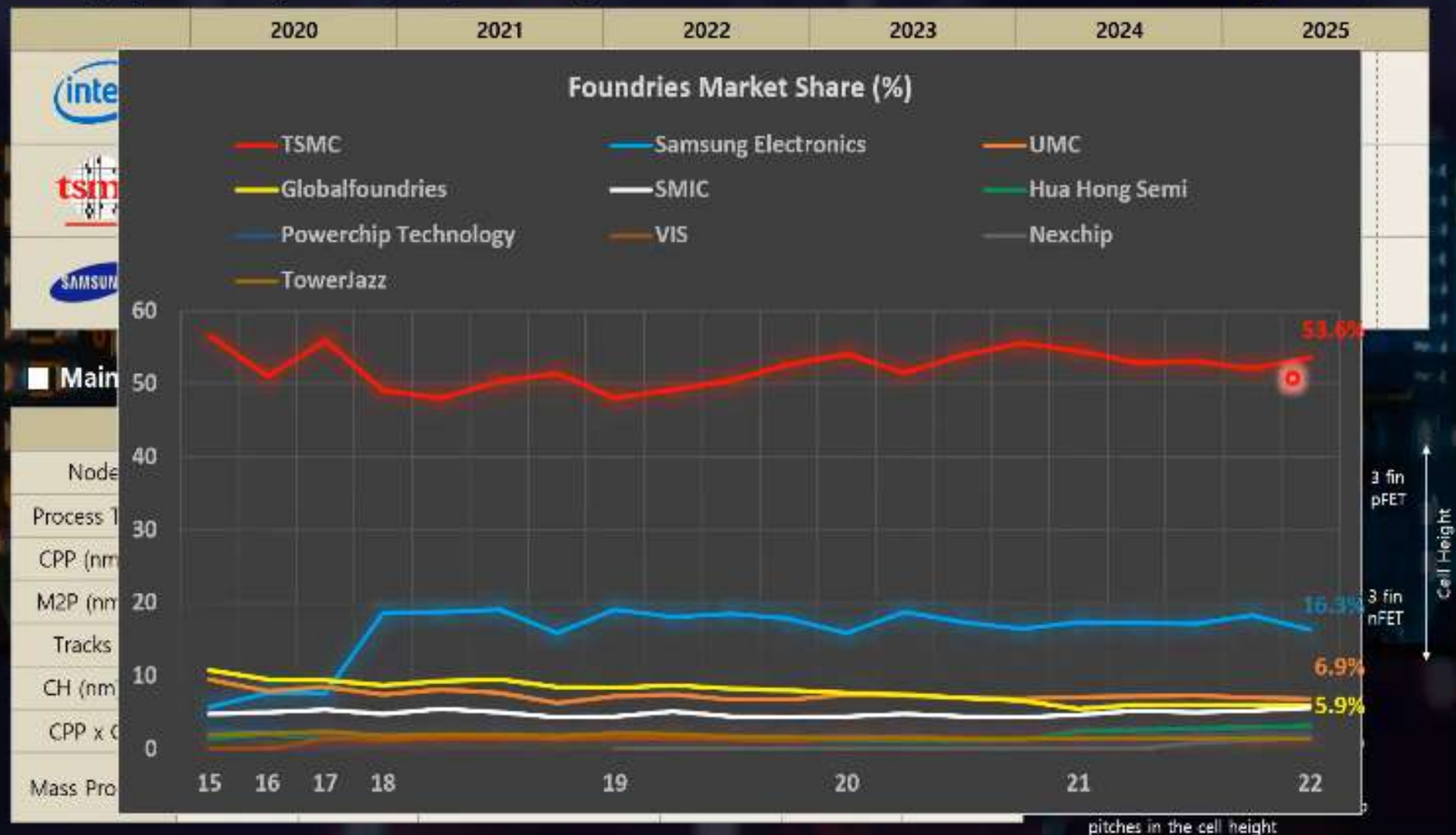
- (1) CPP : Contacted Polysilicon Pitch
- (2) M2P : Metal 2 pitch
- (3) CH (Cell Height) : M2P x Tracks
- (4) Tracks : the number of metal two pitches in the cell height

* source: IC Knowledge, 삼성증권 반도체 투자 보고서

Global Foundry Technology Roadmap

■ Logic process comparison (mass production)

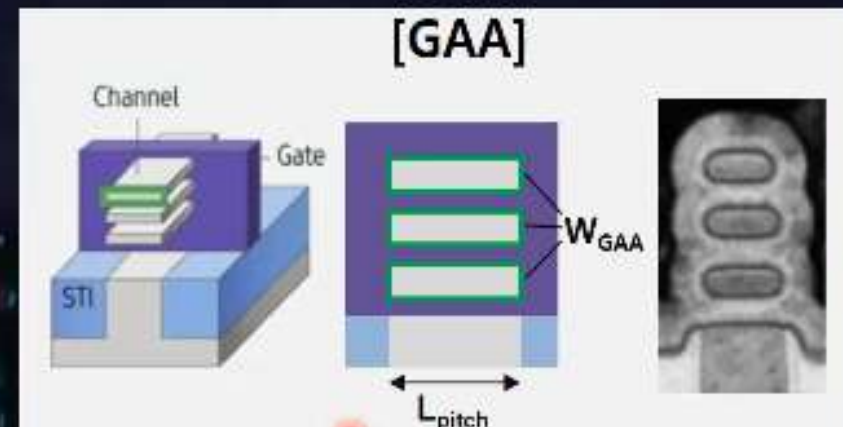
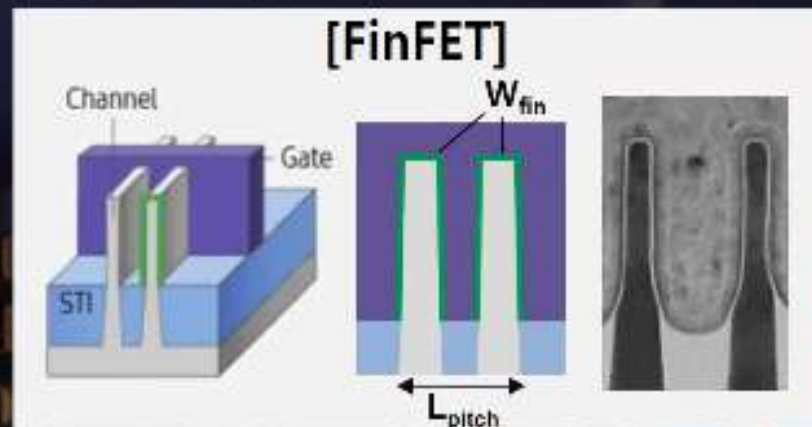
■ FinFET ● GAA



* source: IC Knowledge, 삼성증권 반도체 투자 보고서

FinFET vs GAA (Gate-All-Around)

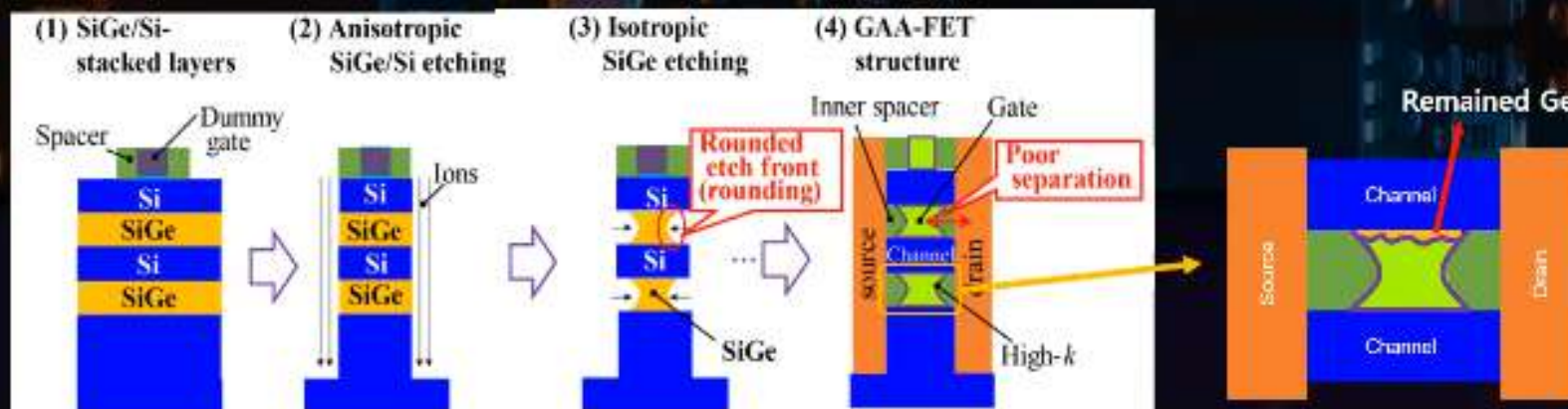
■ Advantage of GAA



- 1) GAA has larger channel width relative to FinFET under the same pitch length (L_{pitch}) condition.
- 2) GAA has flexible control in channel width by changing pitch length (L_{pitch}).

■ Challenge for GAA

※ GAA Process Flow

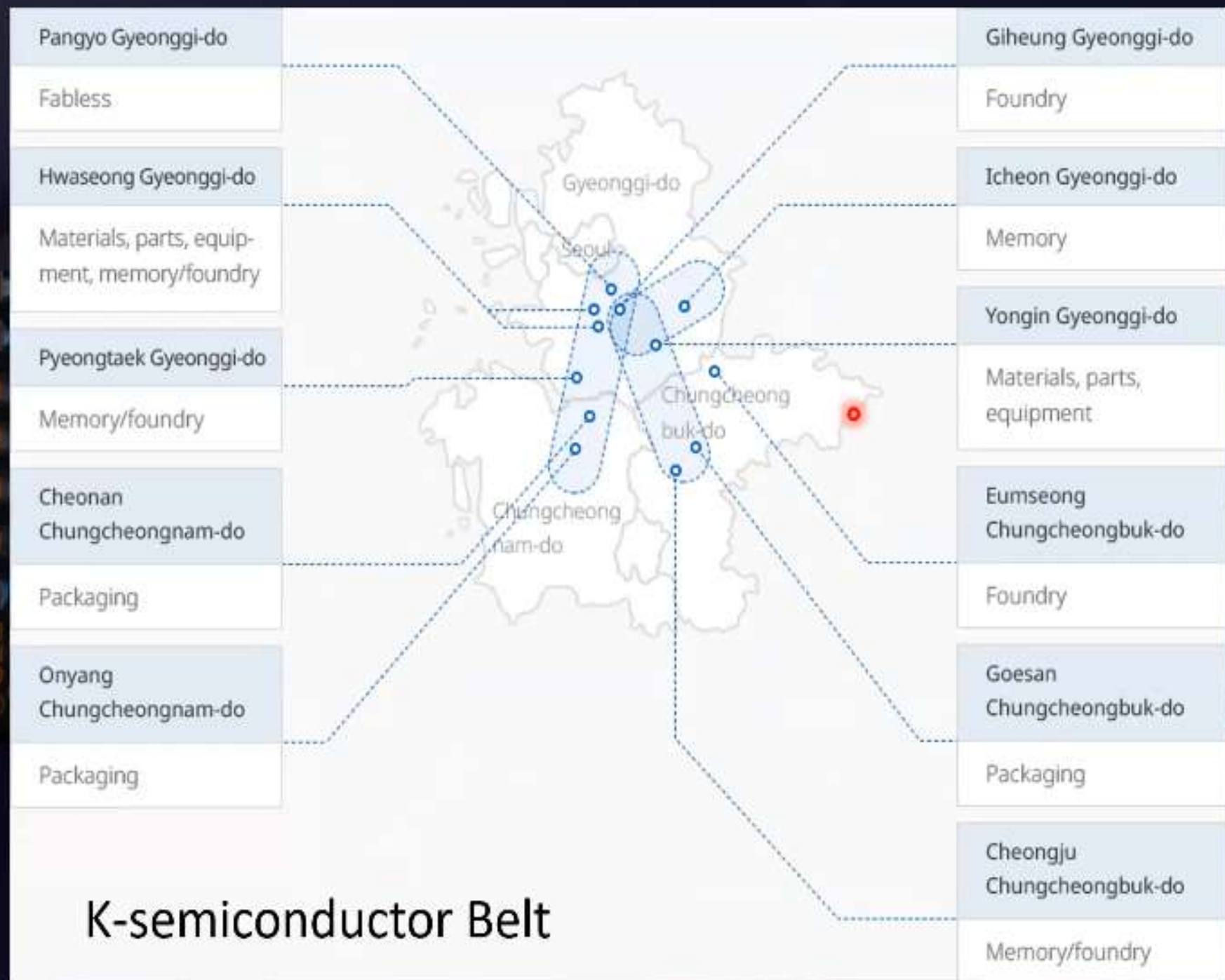


- 1) Stacking uniform multilayer Si/SiGe is challenging due to lattice mismatch control.
- 2) Isotropic lateral SiGe etching is also challenging.
 - Rounded etch front can cause poor physical separation between Source/Drain.
 - Remained Ge can degrade uniformity of High-k gate oxide and cause variation of device characteristic.



CHIP 4 alliance ?

We have already made the decision!



G. I. T. E. (Governance, Infra, Technology, Education)

