New Approach of Chip Manufacturing in China

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Highlight

浙江大学 微纳电子学院
SCHOOL OF MICRO-NANO ELECTRONICS
ZHEJIANG UNIVERSITY

1. Background
2. China Future approach
3. Summary

Background

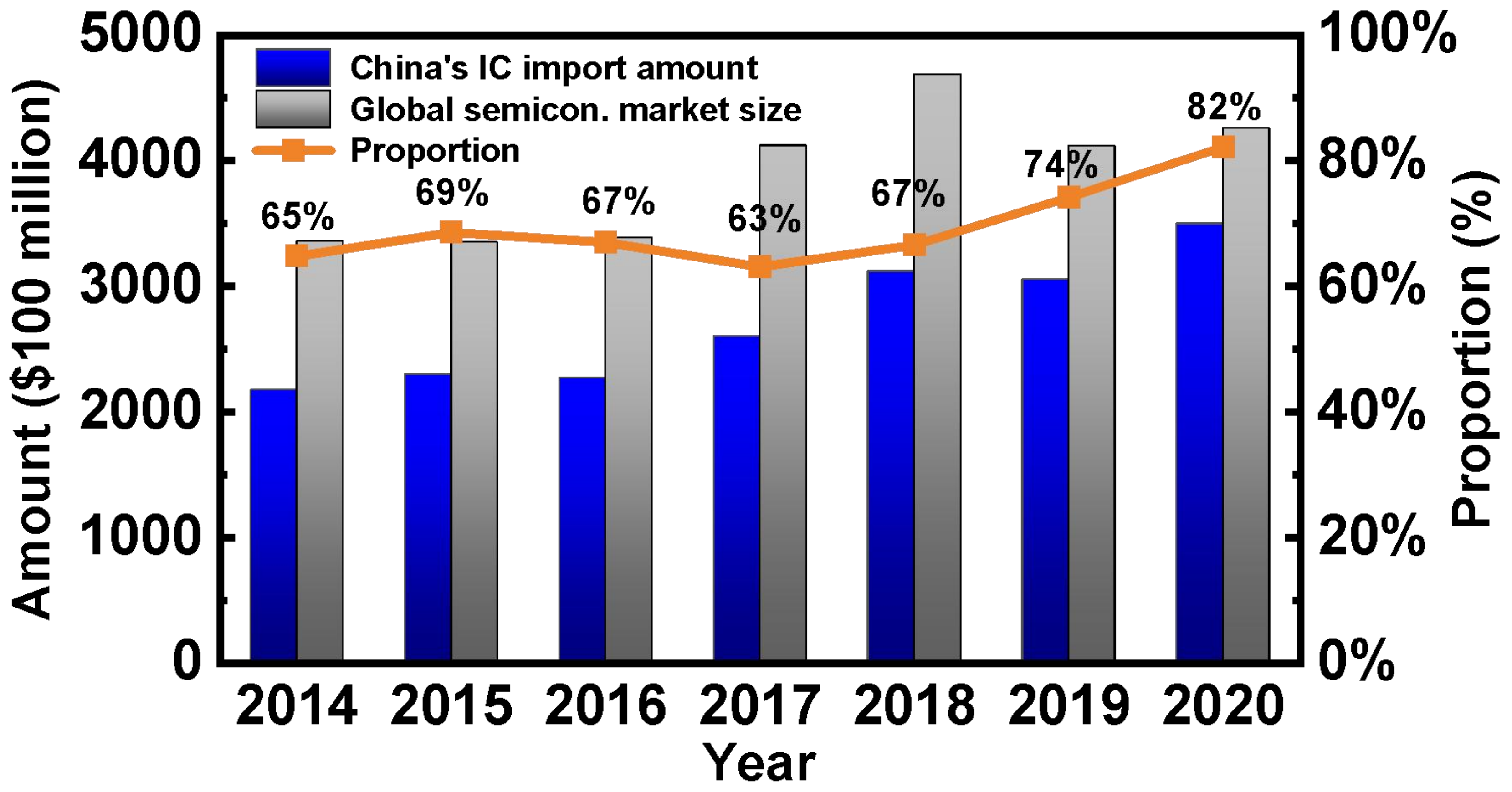
IC in China

Semiconductor
$439.7B

Imported in 2021

Four Strategic materials imported

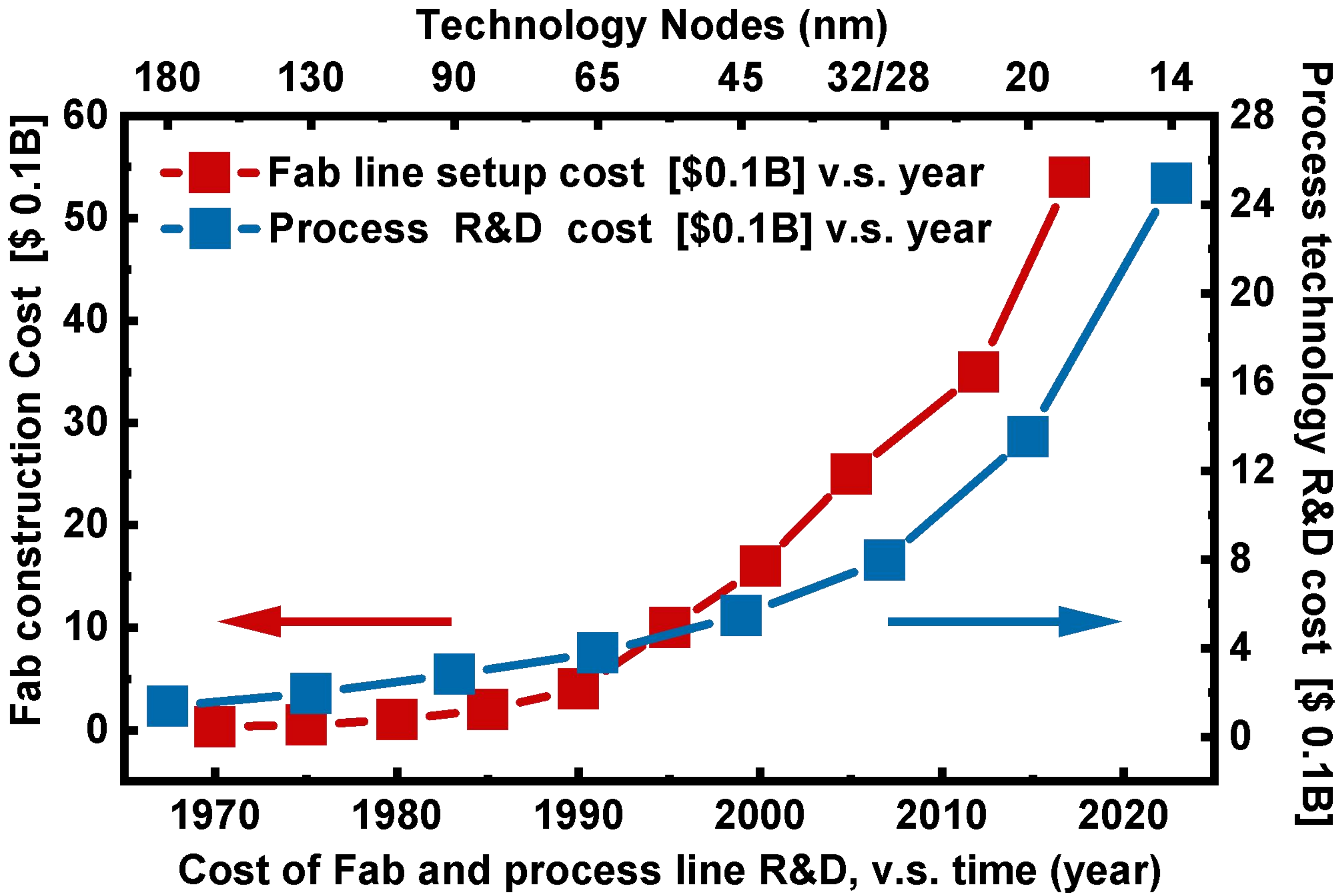
Petroleum | **Ironstone** | **food** | **RefinedOil**



Background

Cost of Advaced Technology Nodes
Fab & R&D

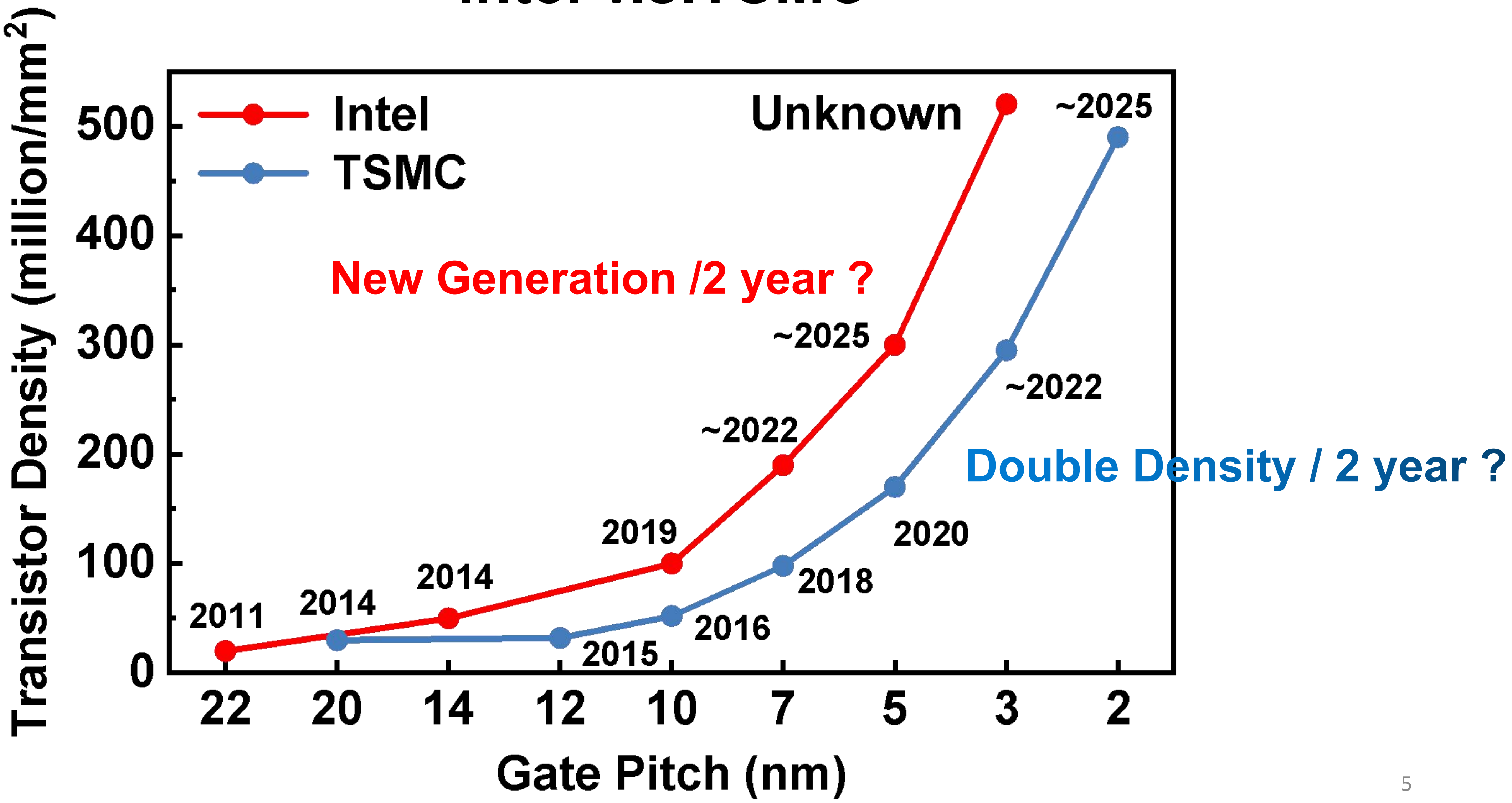
14 nm Fab
cost US$ 6B



14 nm R&D
cost US$ 2B

Background

Intel v.s.TSMC



The Global Semiconductor Supply Chain Based On Geographic Specialization Has Delivered Enormous Value For The Industry

Semiconductor Supply Chain

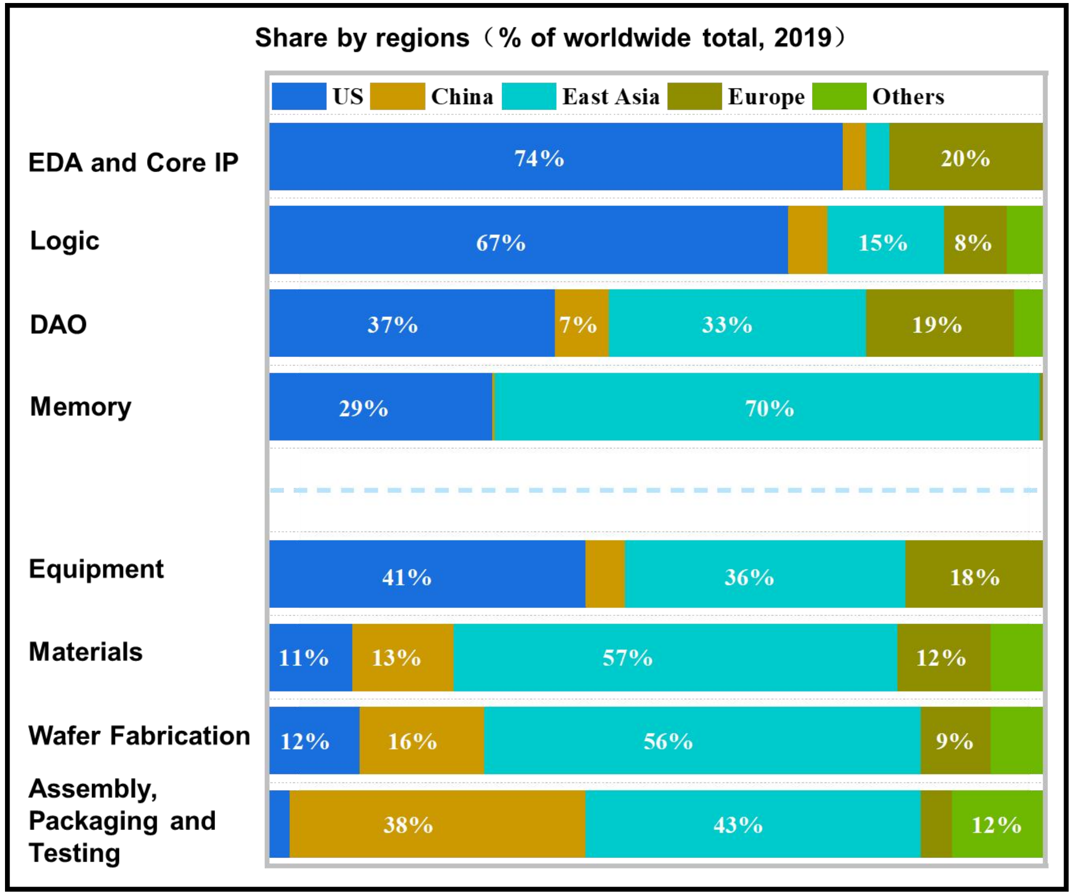
Precompetitive Research

▽

EDA **Core IP**	**Design** • Logic • DAO • Memory

▽

Equipment **Materials**	**Manufacturing** • Wafer fabrication • Assembly, Packaging and testing



Cost savings vs. Fully localized "self-sufficient" Supply chains:

$0.9-1.2 T
Avoided upfront Investment

$45-125 B
Annual cost efficiencies

35-65%
Enabled reduction in semiconductor prices

-From BCG analysis

Background

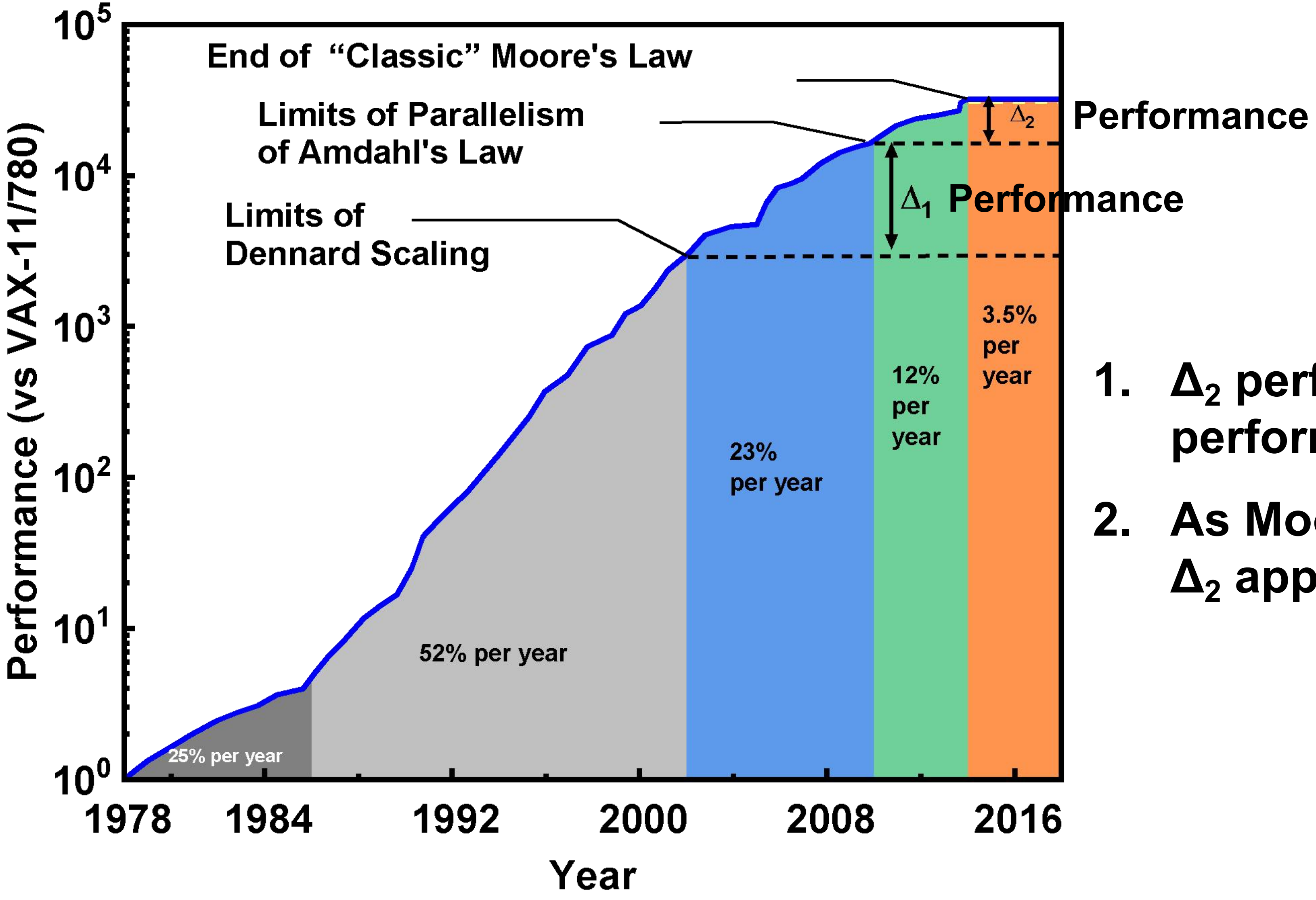
Worldwide Evolution of CMOS Nodes

CMOS Node	65nm	45nm HkMG	32nm (2009)	22nm Tri-Gate (2011)	14 nm FinFET (*IEDM* '14)	10nm (FinFET *IEDM* '17)
L_g (nm)	35	35	30	26	22	20
Contacted Poly Gate/(Metal 0) Pitch (nm)	220	160 **0.703**	112.5 **0.711**	90	70 (56)	54 (36)
SRAM Area (mm^2)	0.57	0.346	0.148	0.092	0.0588	0.0312
n/p-MOS I_{on} mA/mm @ V_{dd}=1V & I_{off}=100nA/mm	1.21/ 0.71	1.36/ 1.07 **length scaling factor**	1.55/ 1.21	1.07/0.85 V_{dd} =0.75V	1.04/1.04 V_{dd}=0.7V (I_{off}=10nA/mm)	1.8/1.5 V_{dd}= 0.7V I_{off}=10nA /mm

Tsinghua Uni. Prof. Zhiping Yu

Background

Slow Down Moore's Law Provide an Opportunity



1. Δ_2 performance < Δ_1 performance
2. As Moore's law slows down, Δ_2 approaches 0

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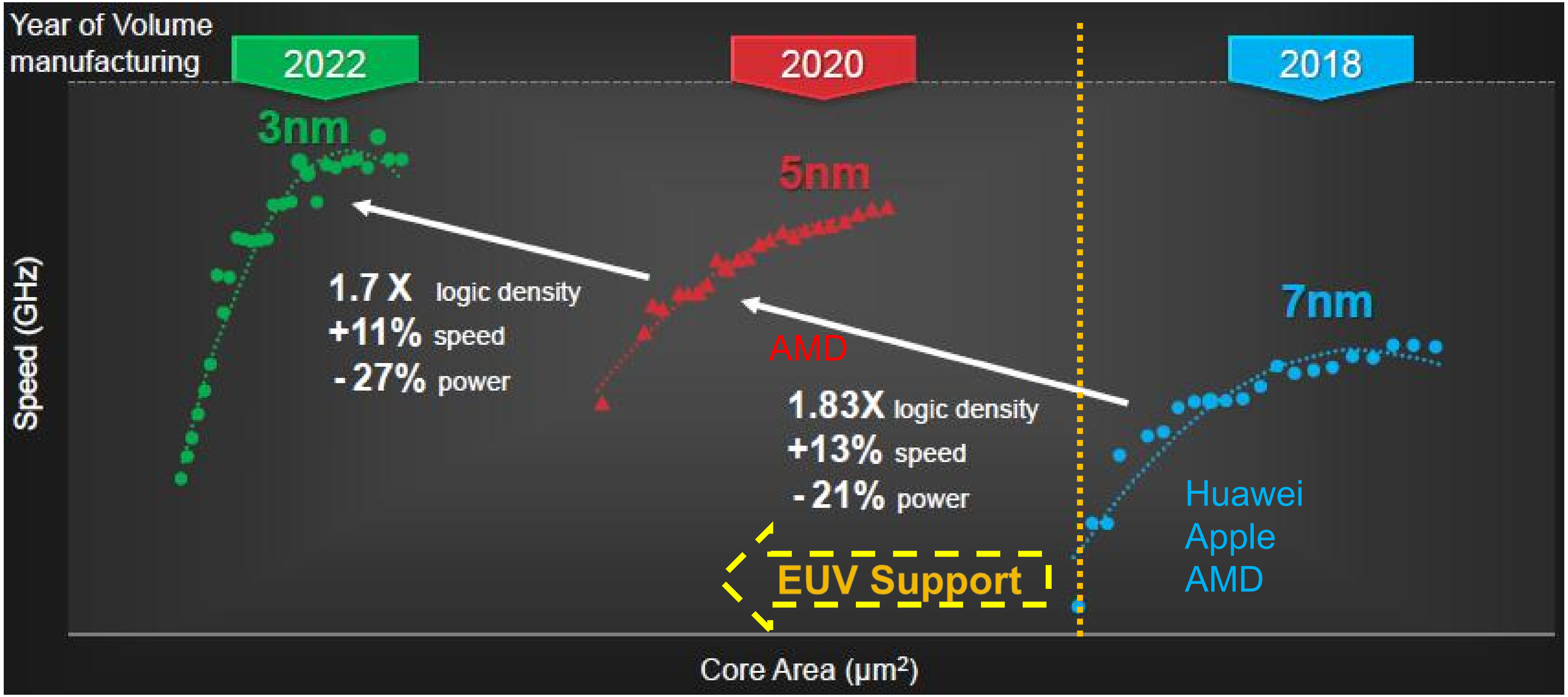
Manuefacturing Technology in China Mainland

1. 28/14nm manufacturing processes for some special products is ready
2. 300mm wafer start to provide to chip manufacturing fab
3. Some key process equipments, such as advaced plasma etch tools, are technically ready to support chip manufactruing
4. Specialized CPU and 5G chips can be made in local chip Feb.

From :https://www.163.com/dy/article/HHE8F40E055225XN.html

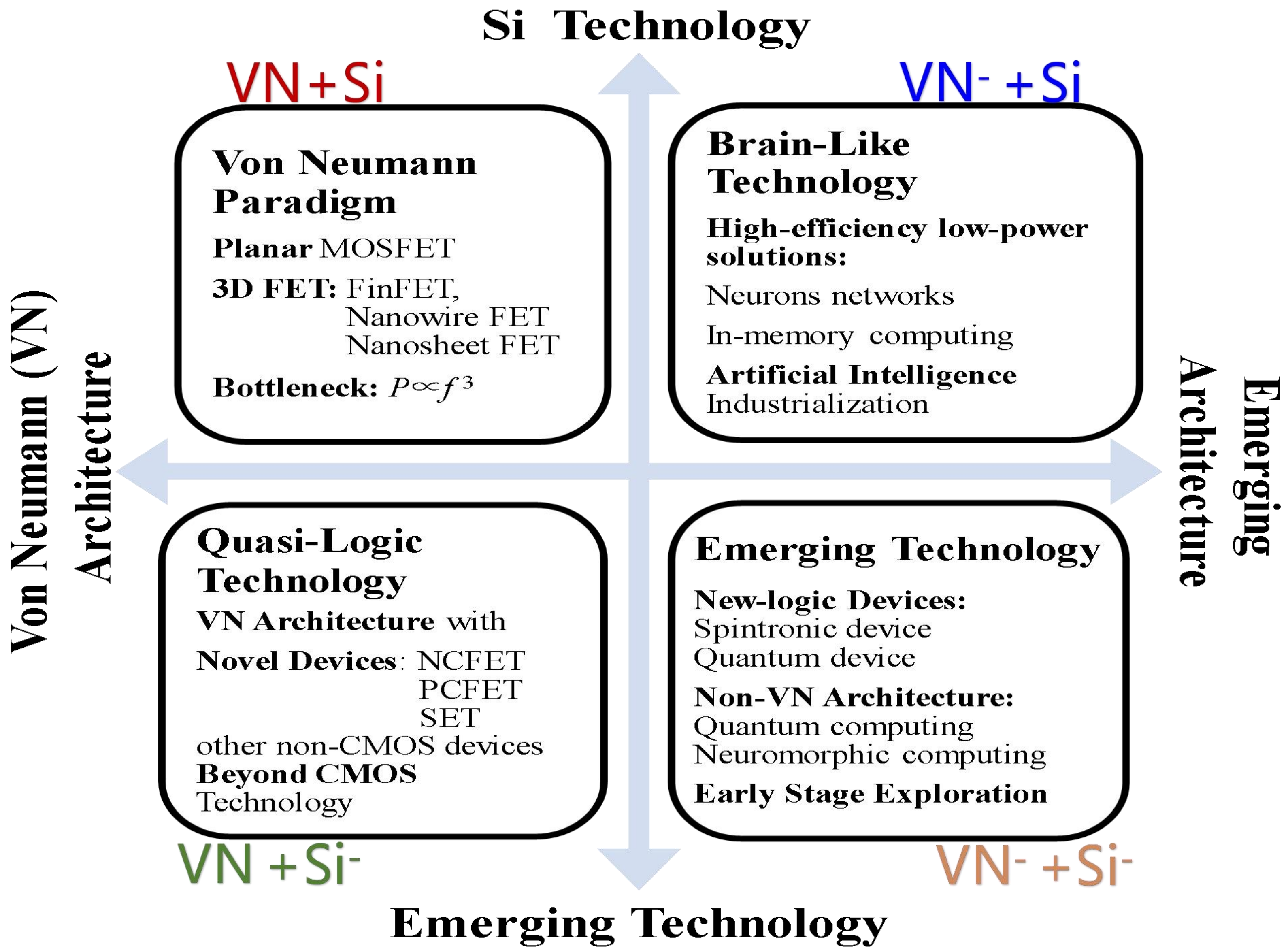
TSMC Technology Roadmap

- Fine Feature size (TSMC, *ISSCC* 2021)



Tsinghua Univ. Prof. Zhiping YU

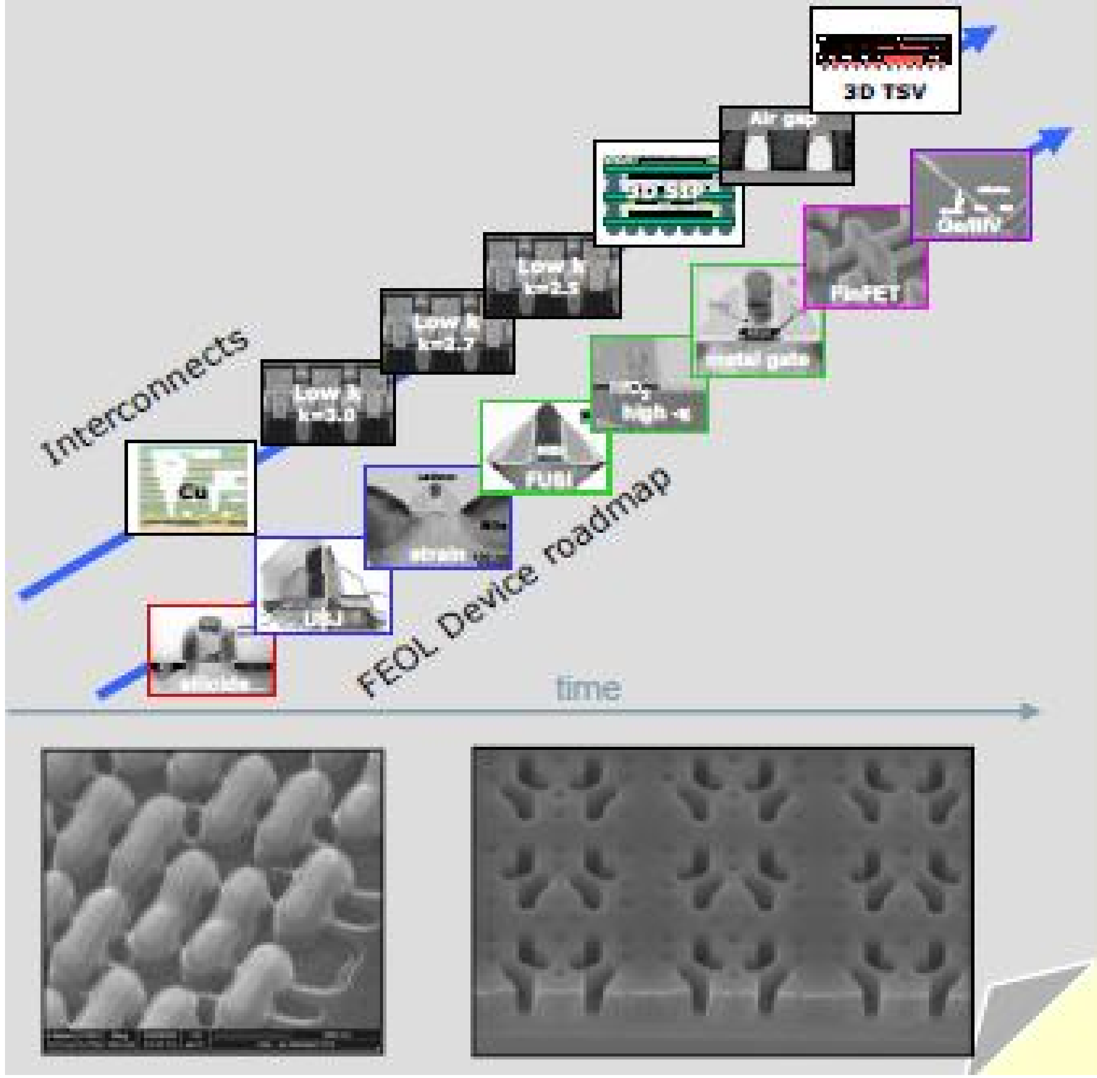
Technology Trends for Future Applications（Quadrant)



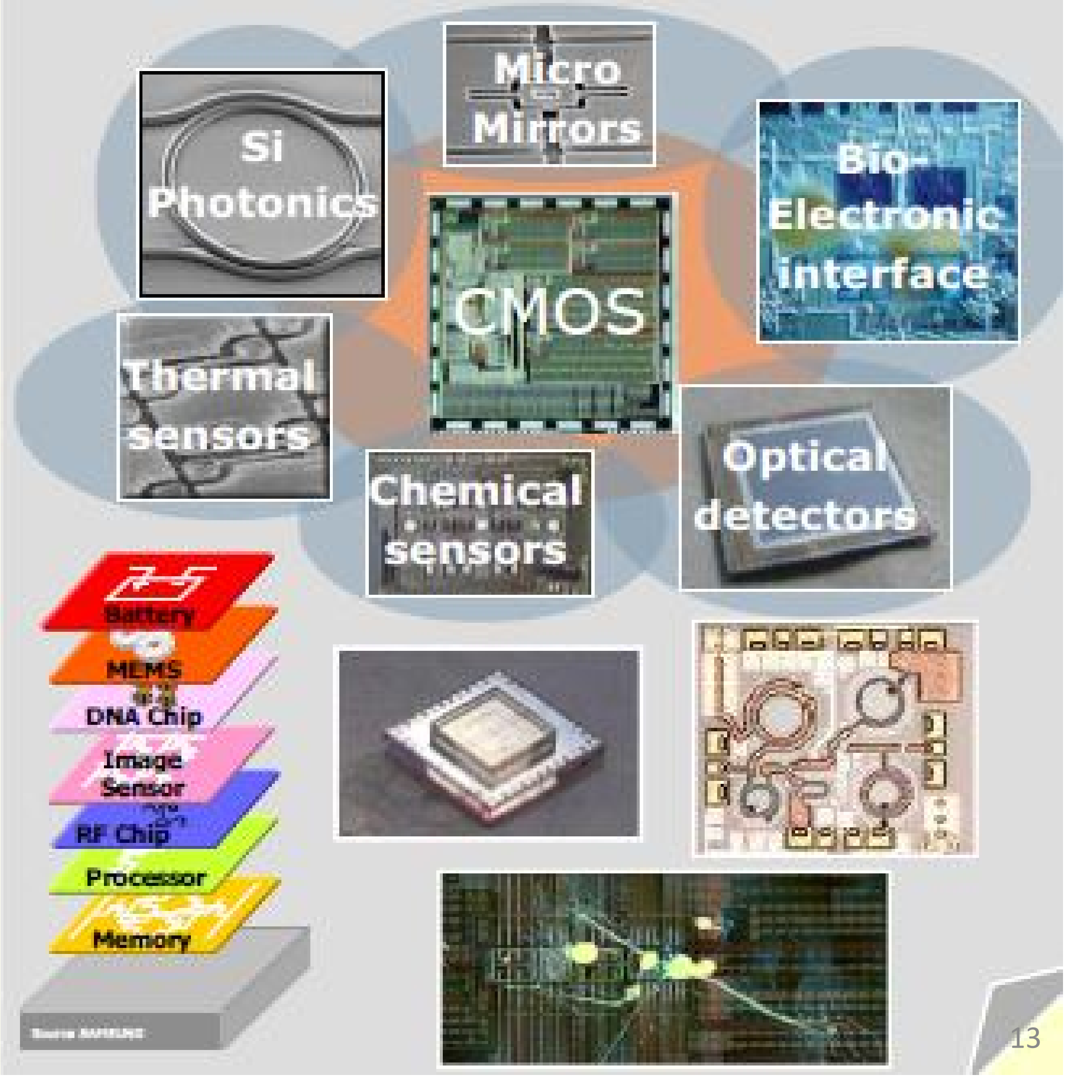
Two Major Technology Approaches

From IMEC

More Moore



More than Moore



Post-Moore's Technology Trend

Market Driven

•HiSpd Computing

•Mobile Computing

•Autonomous perception & Calculation (IoT)

Technology

- Logic technologies
- Ground rule scaling
- Performance boosters
- Performance-power-area (PPA) scaling
- 3D integration
- Memory technologies
- DRAM technologies
- Flash technologies
- Emerging non-volatile-memory (NVM) technologies

PPAC Next Target in 2~3 years

(P) Performance: Frequency raise 15%@ Voltage

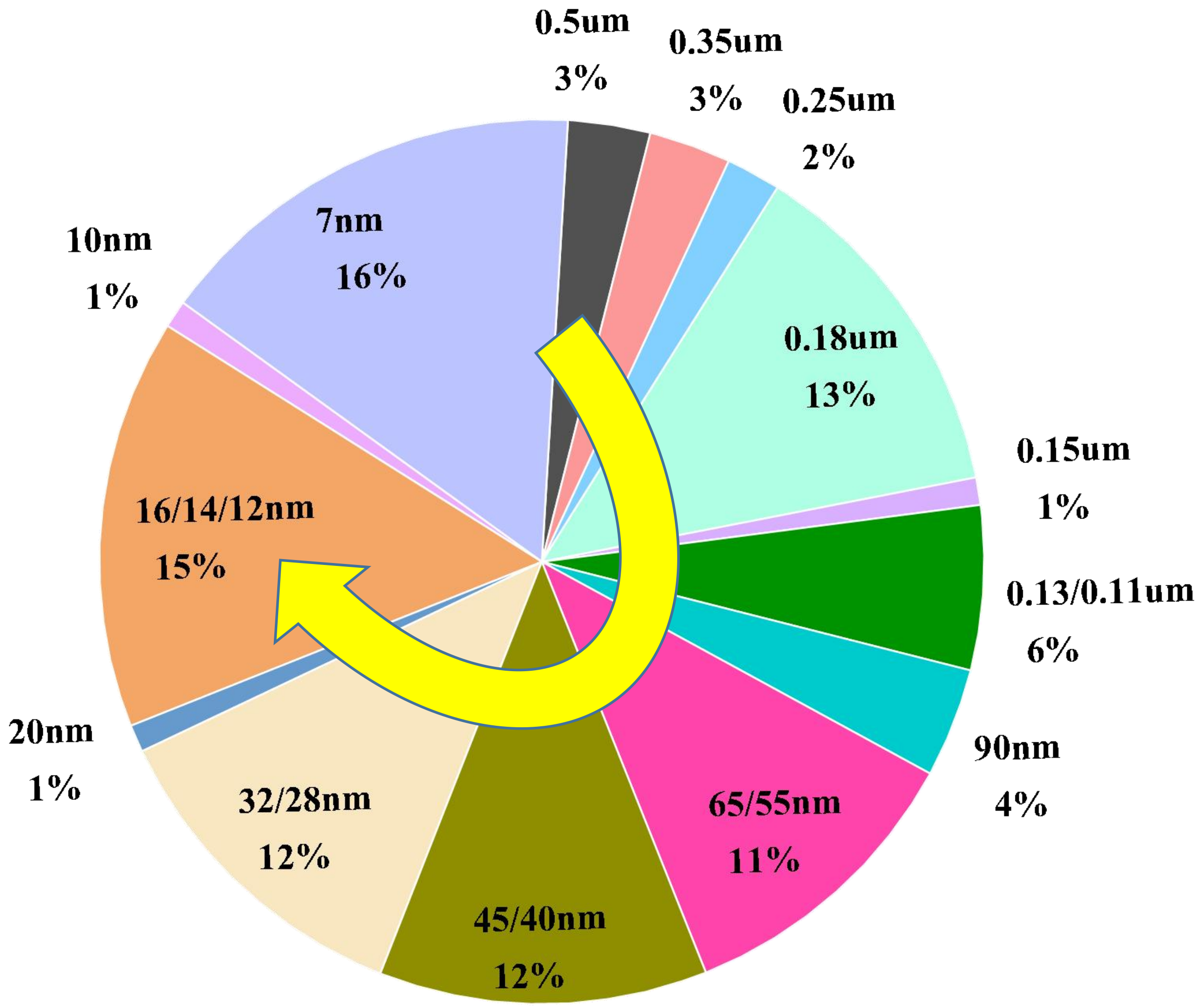
(P) Power: Reduce>30%@Same performance

(A) Area: Reduce 30%chip area;

(C) Cost: Wafer raise < 30% -Unit cost reduce 15%

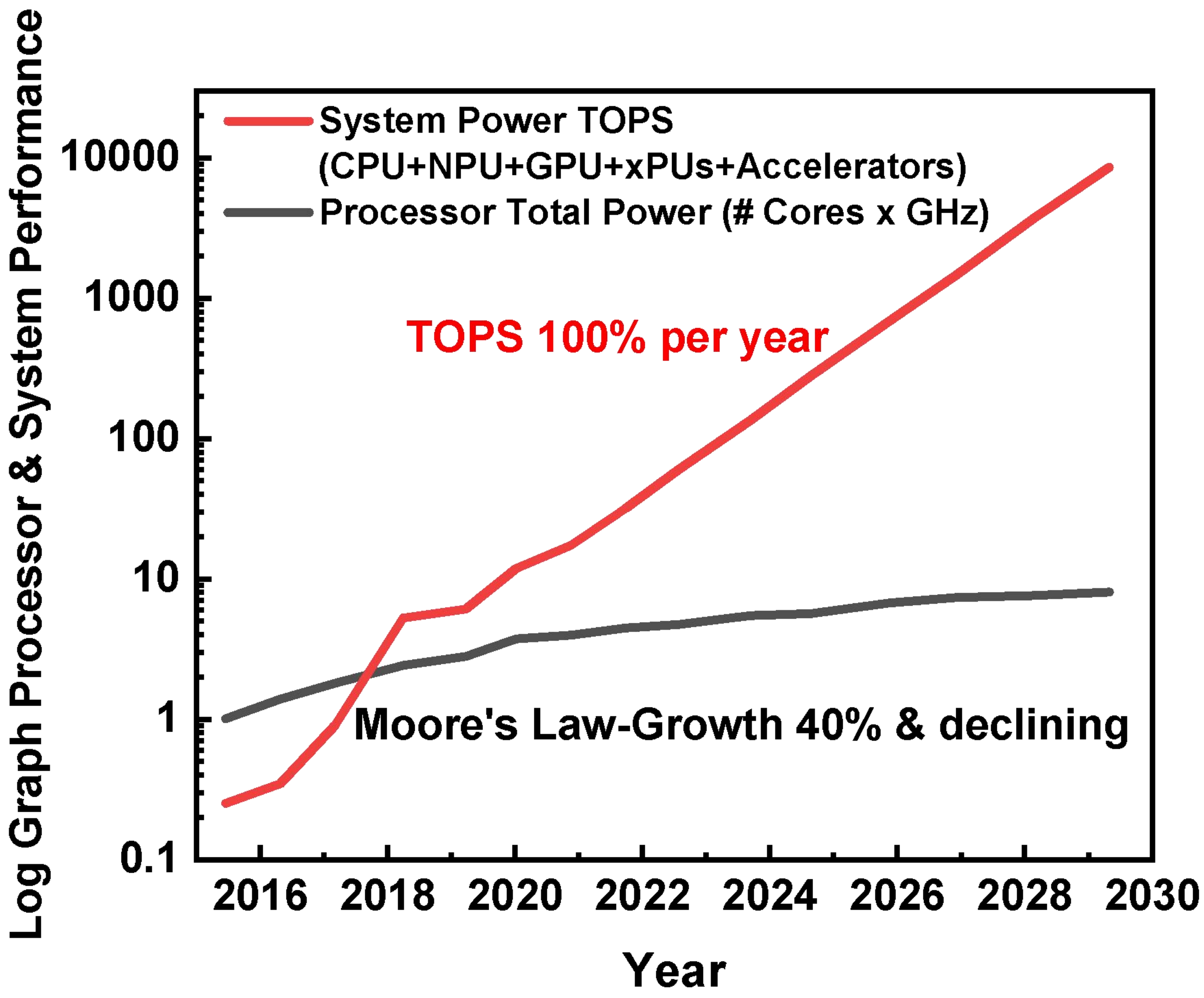
Large Market Share in Matured Technology

- 83% market share at nodes above 10 nm
- Great room for innovation



From Industrial Securities

IC Technology Advancement Cannot Support The Increasing Demand in Computing Capability



How to meet
the huge demands
of computing capacity ?

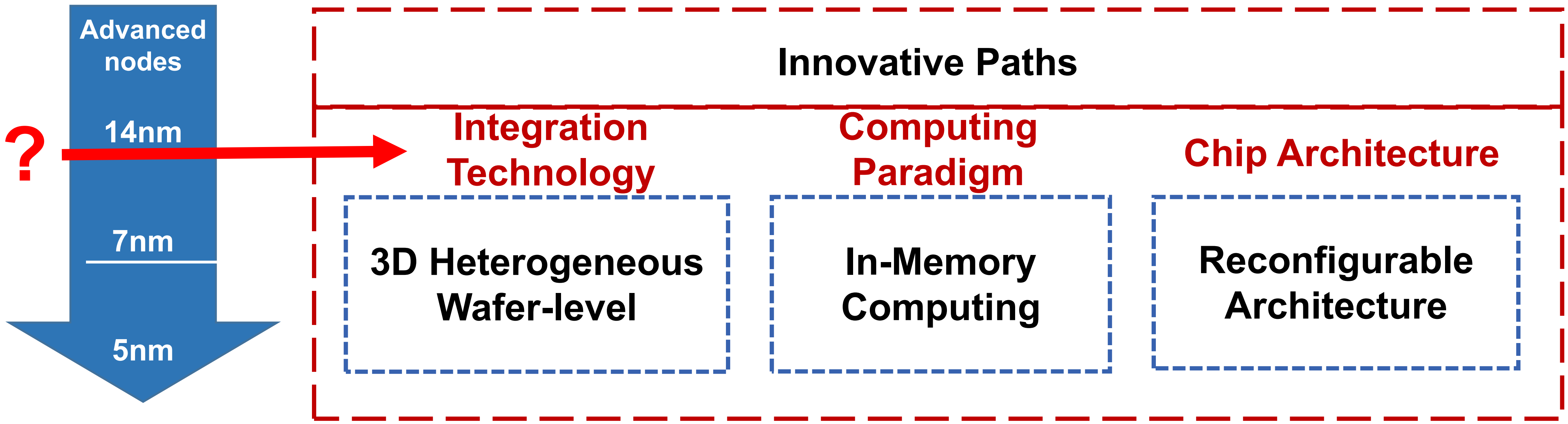
From Wikibon Analysis 2021

Future Trends for High Computing Capability Innovations

High computing capability can be achieved by innovations on computing paradigm, chip architecture, and integration technology

Computing Capability (CC) ~ transistor number (millions) × CC/million transistors

Increase the number of transistors	Increase computing capa. / million transistors



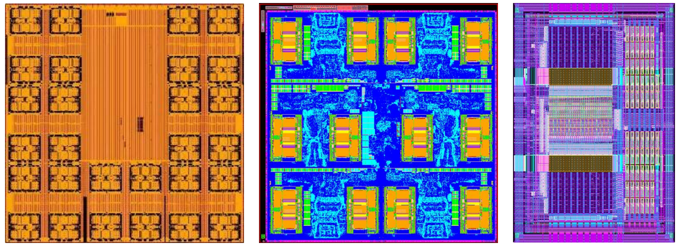
Increased Computing Capability in the Chips

Tsinghua Uni. Prof. Huaqiang Wu

Future Trends for High Computing Capability Innovations

Computing-in-memory Chips

64 MB (world's largest) computing-in-memory chip featuring 28 nm technology node and 300-500 TOPS

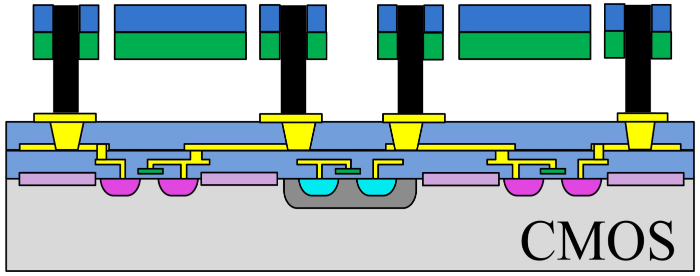


Reconfigurable Chips

Mixed-grain reconfigurable processing unit featuring 40 nm technology node and the world-leading energy efficiency (~20TOPS/W)

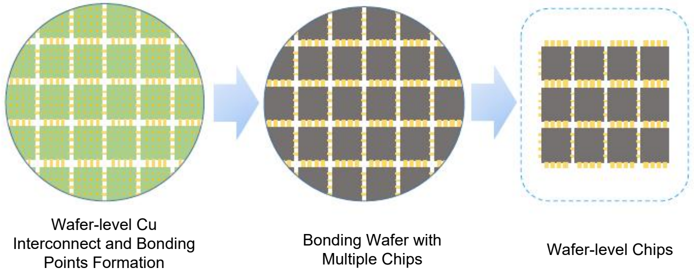
3D Integration Technology

TSV-based 3D heterogeneous integration has been demonstrated



Wafer-level Integration

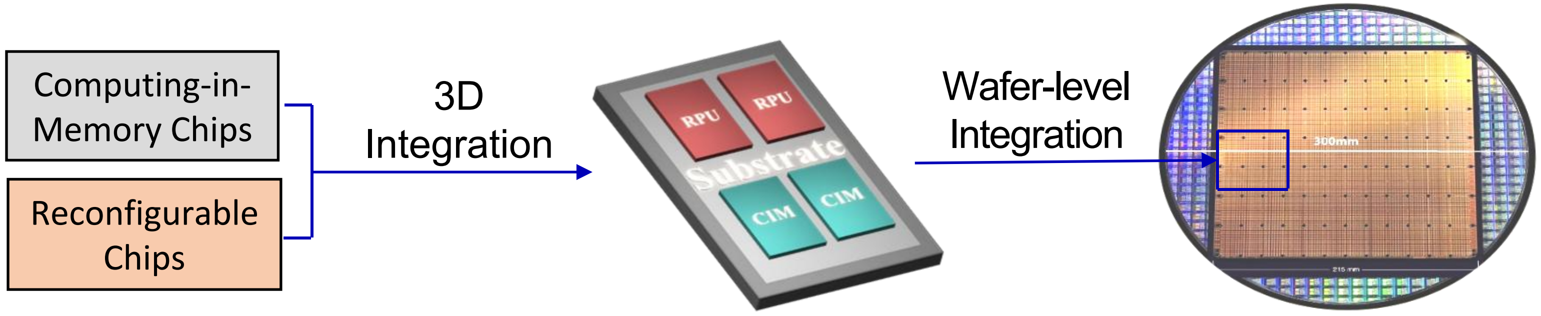
Multiple patterning technology for interconnect fabrication with large node technology



Suggestions

1~2 Years

3~4 Years

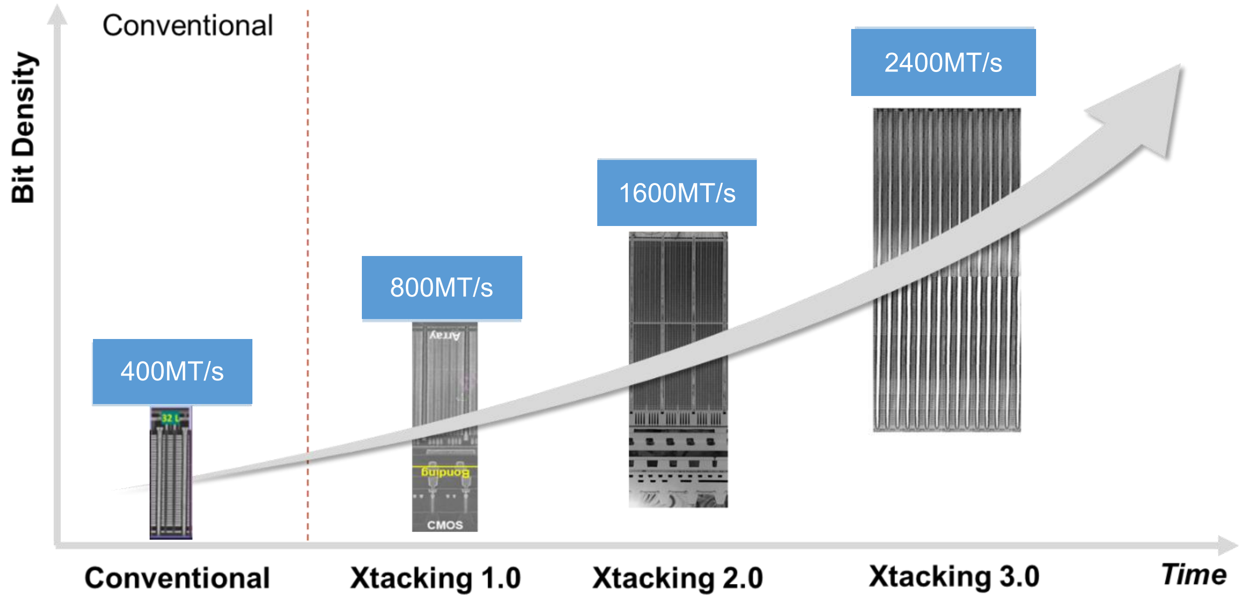


Tsinghua Uni. Prof. Huaqiang Wu

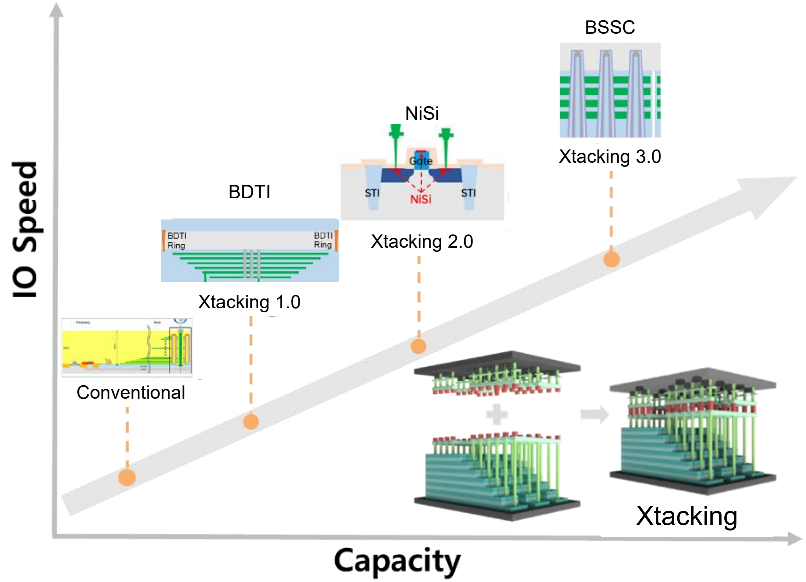
Xtacking: From Revolution to Evolution:

To achieve higher density, higher speed and fast TTM,
new innovations has been introduced to address the challenges along with the vertical scaling.

In the pursuit of higher density

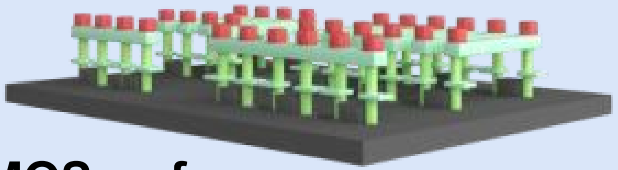


Evolution driven by innovations

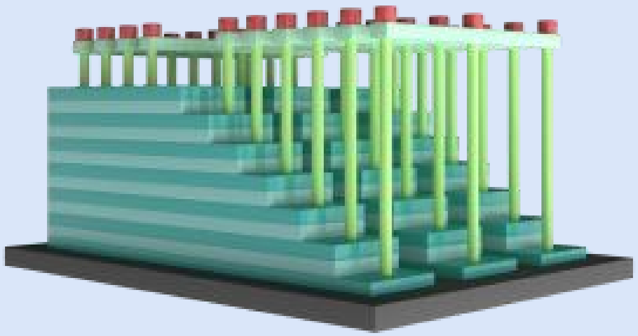


Xtacking™ Concept

Independent processing
On separated wafers

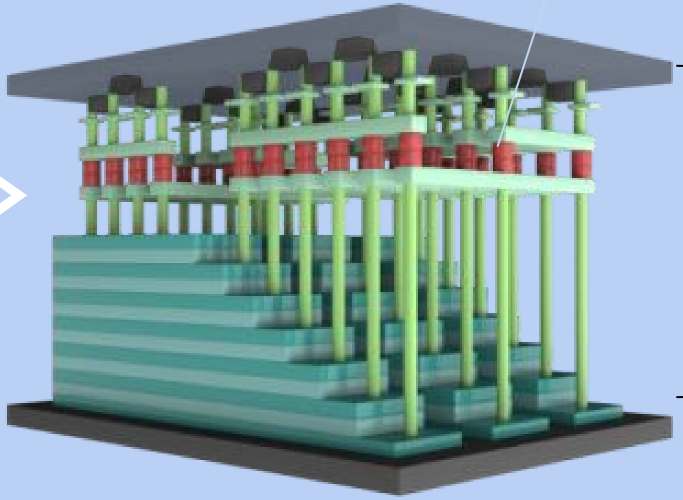


CMOS wafer



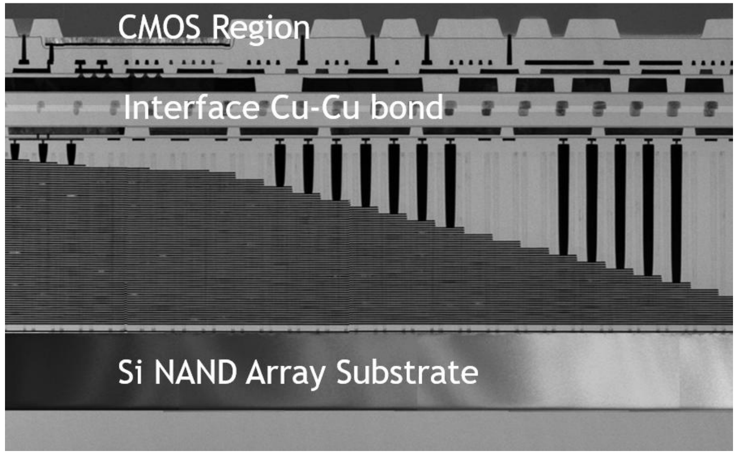
Memory cell wafer

Wafer bonding processing
with millions of metal **VIAs**
(Vertical Interconnect Accesses)



Into one wafer

Xtacking™ architecture



FMS 2018

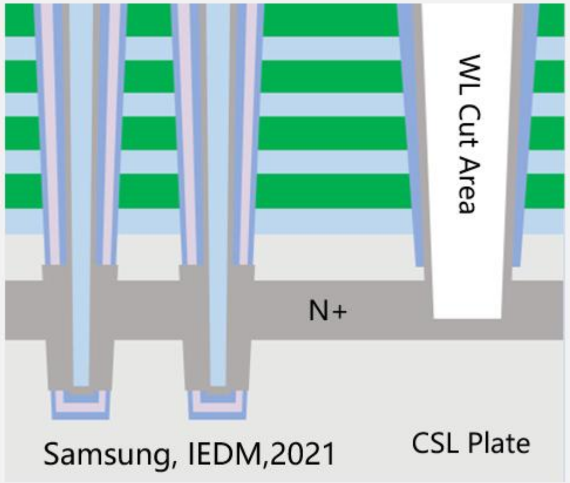
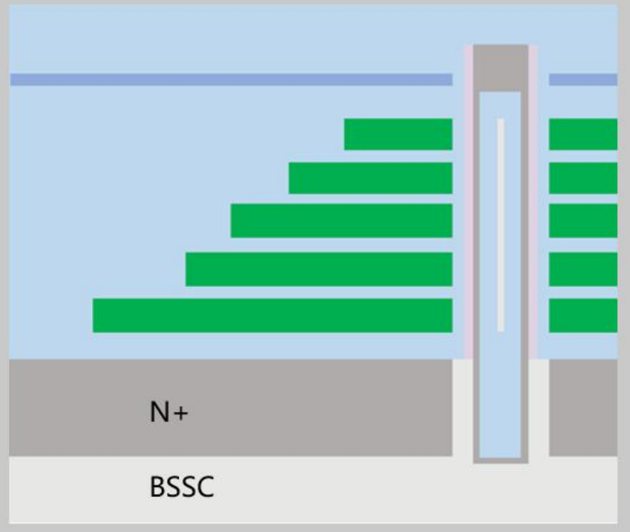
Higher IO speed
Up to 3.0Gbps IO speed

Higher bit density
CMOS Array hybrid bonding enhances Array Efficiency

Faster time-to-market
Modularized, parallel approach to product development and manufacturing

Xtacking® 3.0 with BSSC

- BSSC (Back Side Source Connect) in Xtacking®: Simple process, lower cost and much lower defect level
- Transition from front side deep trench process to back side surface process – **much faster yield learning curve**

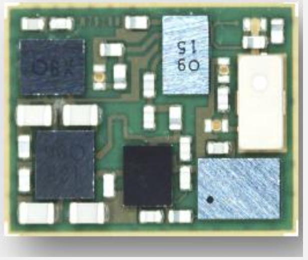
Category	CSOB (Channel-hole Sidewall ONO Butting)	BSSC (back-side source connection)
Structure		

Simple process and low cost

FMS 2022

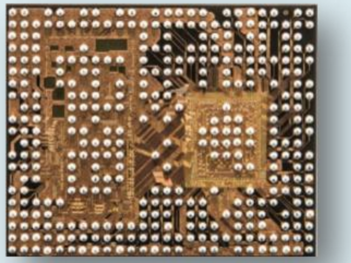
JCET Group Technology Portfolio

- Comprehensive R&D and mass production experiences in conventional and advanced packaging
- JCET Group’s technologies and services have been recognized by the world's leading customers

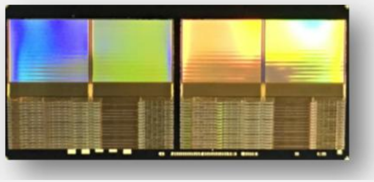


Laminate fcCSP, PoP & SiP

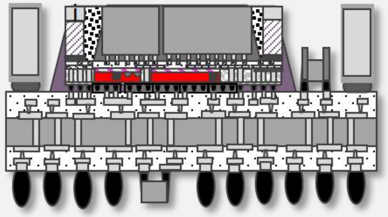
Large-sized fcBGA & SiP



Wafer Level Packaging



Multi-chip Stacked 3D Memory



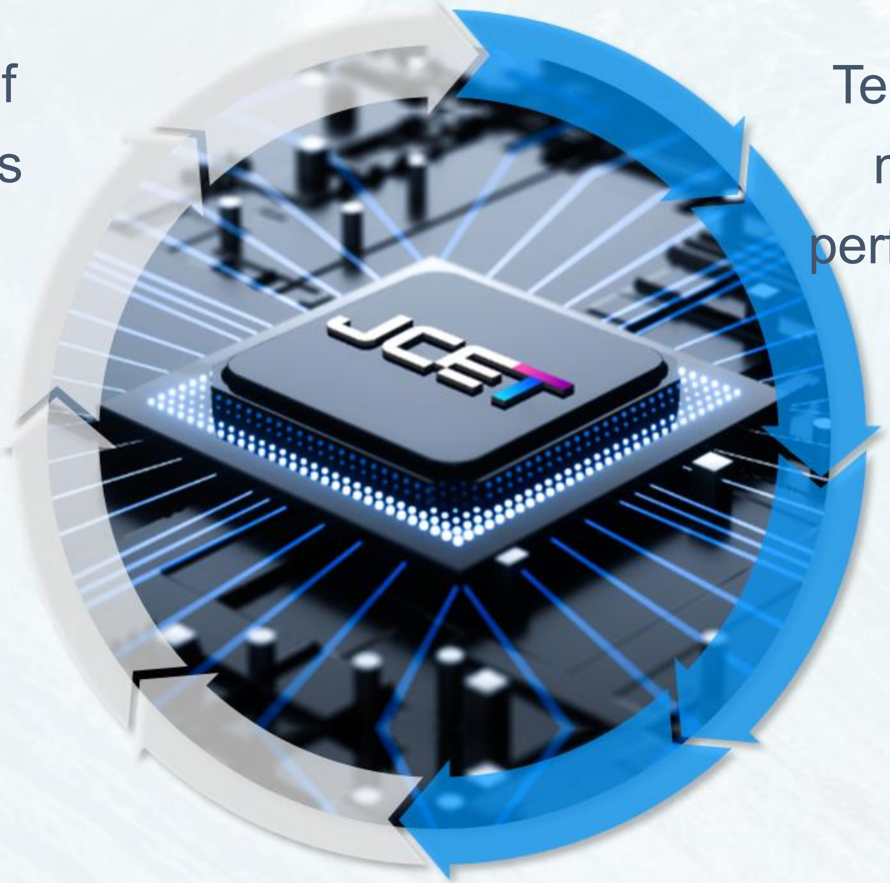
XDFOI™ 2D/2.5D/3D Chiplet

From JCET

JCET Group Technology Development Directions

Accelerate the R&D and MP of high-performance technologies incl. 2.5D and 3D

Technology development for new markets incl. automotive, high-performance storage & computing



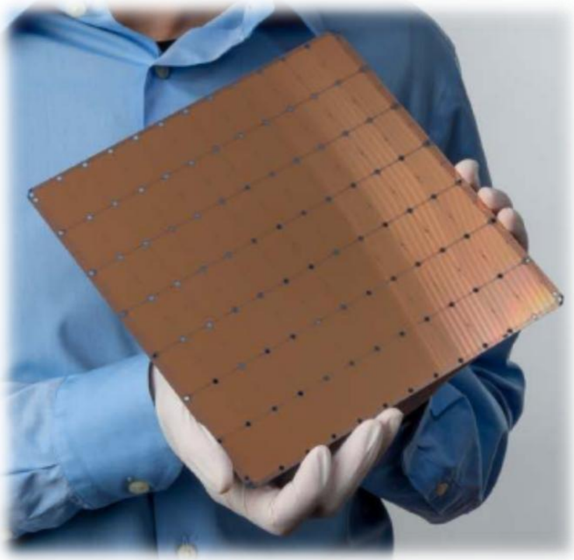
Enhance technical value-added services such as high-end testing and design services

Promote the implementation of intelligent manufacturing

From JCET

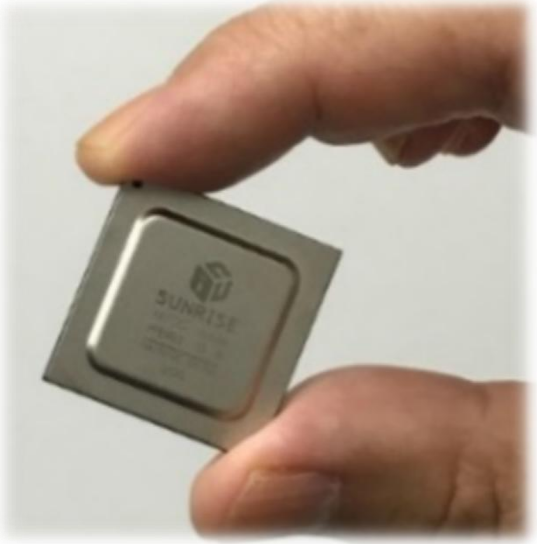
Heterogeneous Integration Technology On Chip (HITOC)

Traditional Achitecture



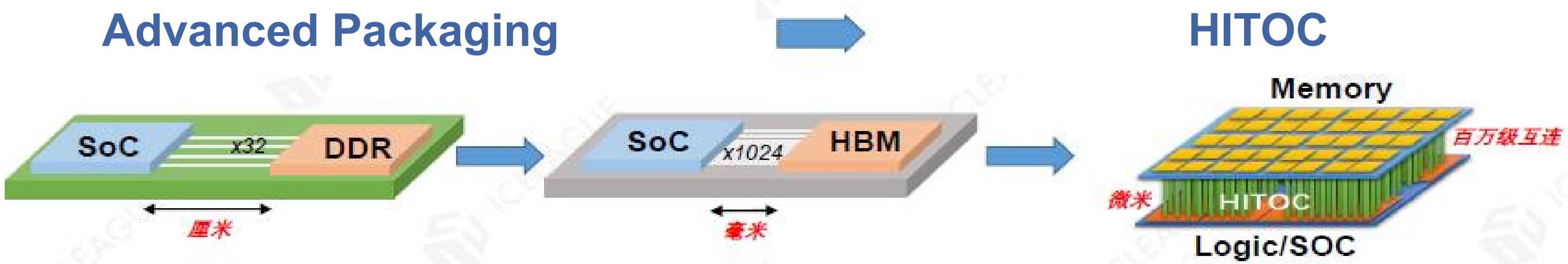
Chips from Corporation C*:
18 GB, one wafer (46,225 mm²)
16 nm Technology Node

HITOC

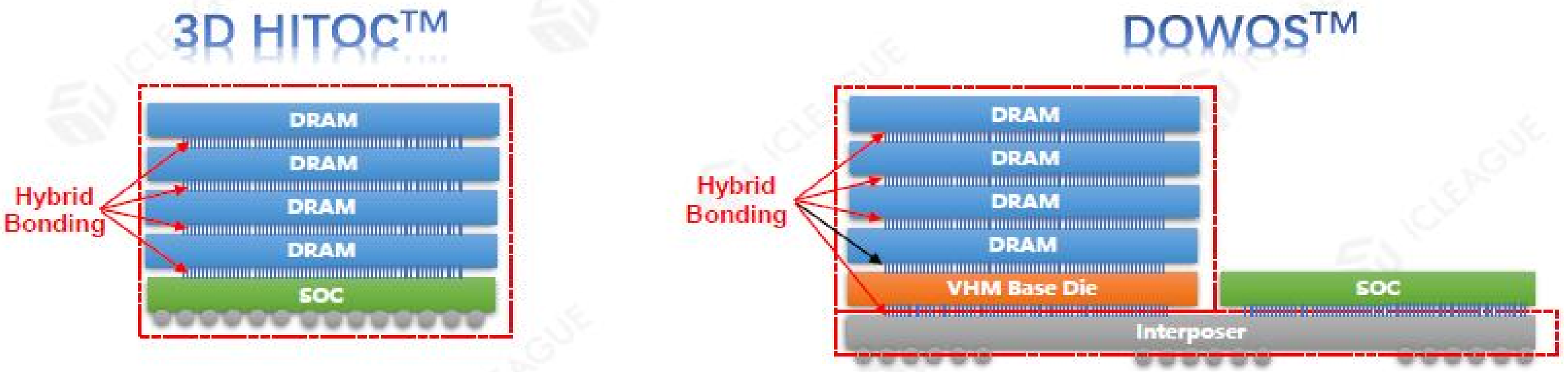


Chip from ICLEAGUE:
19.8 GB, one die (800 mm²)
40 nm Technology Node
Scalable on Demand

Heterogeneous Integration Technology On Chip (HITOC)



HITOC exhibits advantages in performance, power consumption, area, bandwidth, latency, and fabrication simplicity etc.



CSTIC 2022:

- Nano Lab and ICLEAGUE co-invented the large-capacity 3D memory-integrated chip "**Cuckoo**"
- 800mm^2 area, Heterogeneous multi core processor, Intgelligent-NOC, Distributed SRAM, High bandwidth low latency 3D DRAM, 6 GB capacity, 6TB/s memory bandwidth

From ICLEAGUE Feng HONG

The Success of Technology Transformations Based on Integration of Industry & Education

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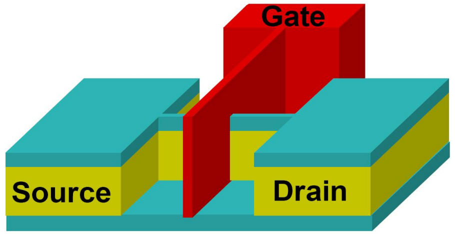
FinFET



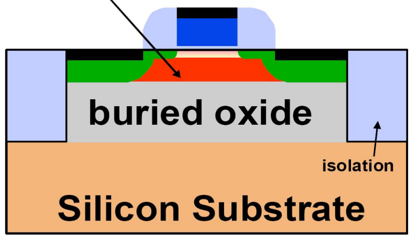
Berkeley ➡ Intel

HK/MG

- Gate dielectric and thickness
- Increase Leakage current
- Reduce reliability
- High k gate dielectric

Yale ➡ TI

Strained Si



MIT ➡ Intel

Raised S/D

- SCE & Series resistance
- Contact resistance
- Ultra shallow junction technology
- Raised S/D, Schottky S/D, etc

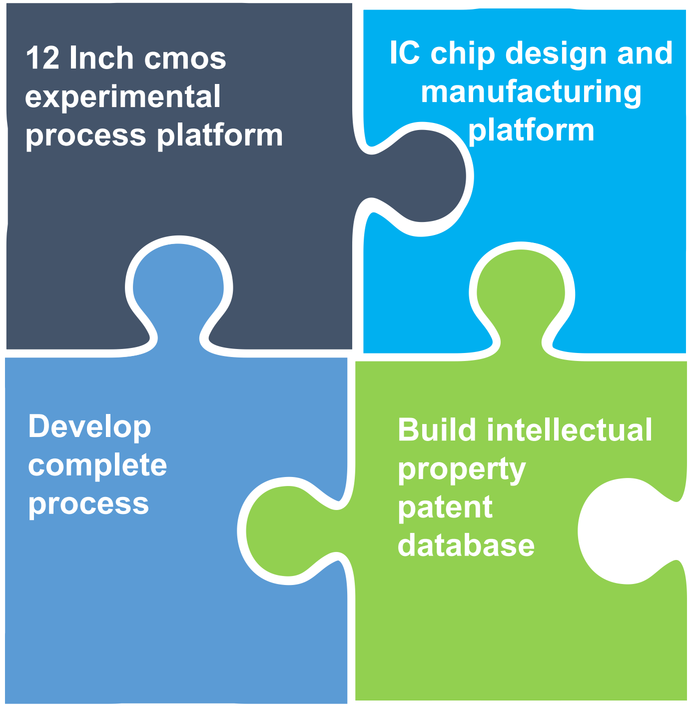
IBM ➡ IBM

It takes more than ten years to transfer the achievement to industry

Three Major Functions of The Platform with a Complete Process Flow

Co-innovation

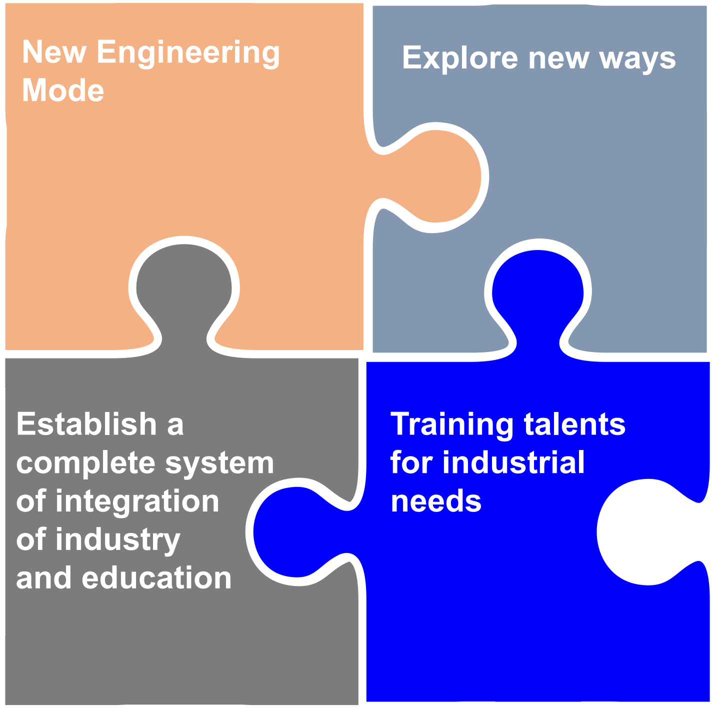
Design-manufacture combination platform



- ✓ 55 nm 12 inch process line
- ✓ For the post moore fragmentation Market

Talent training

Reconstruction of engineering college with combo of industry & Edu



- ✓ New engineering: training of excellent engineers
- ✓ Integration between industry and education

Ecosystem

IC chain construction

- ✓ Complete process verification for equipment and material
- ✓ Incubate innovative enterprises

R&D Mini Line With Complete Process Flow at ZJU

July 2021,Roof-sealing **The end of 2021,Main body completion** **April 2022,Tape-out**

September 2022,Wafer out

R&D Mini Line With Complete Process Flow at ZJU

April 2022 all tools moved in

Full Process Flow Pilot Platform For Interdisciplinary Transformation To Industrialization

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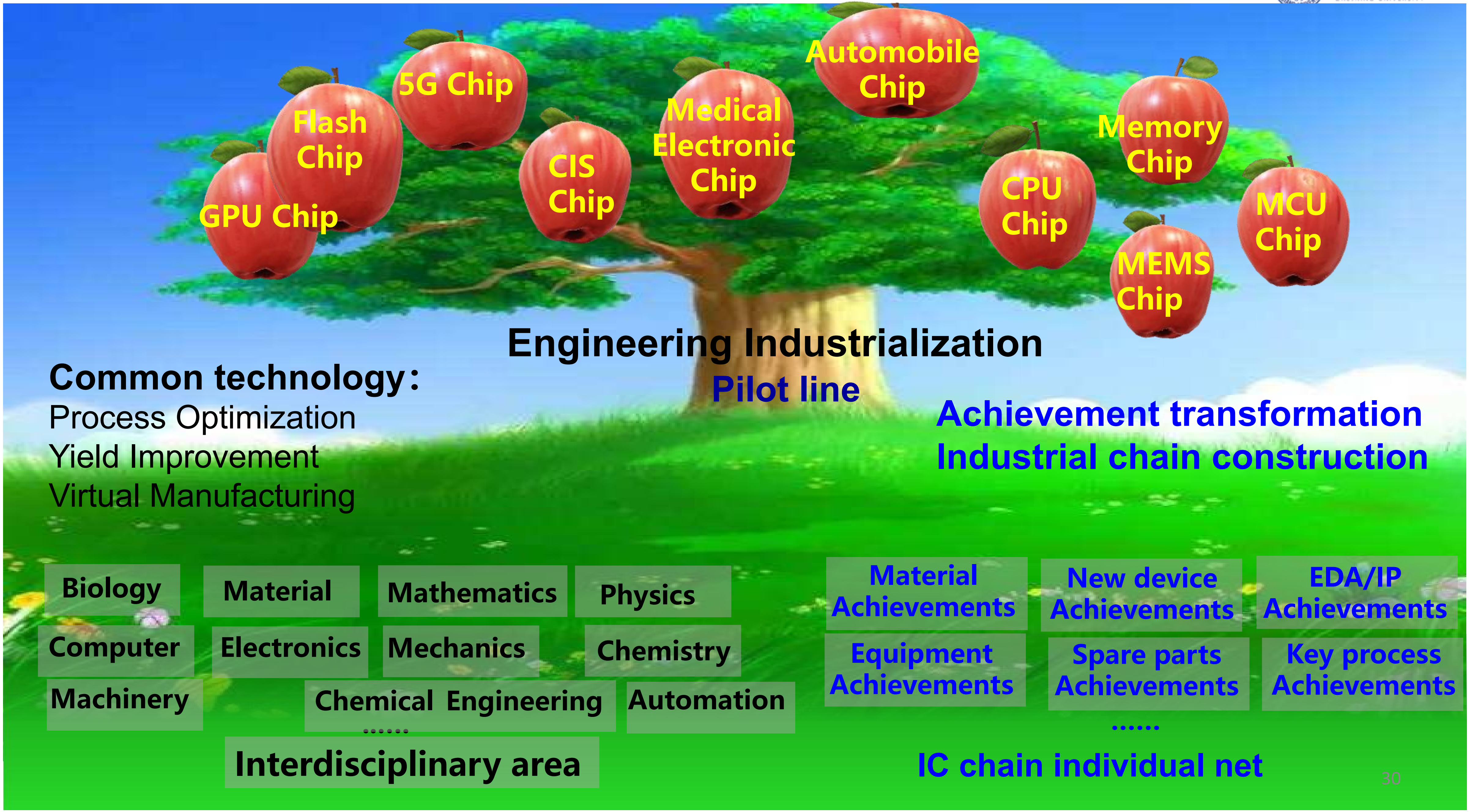

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Summary

- Advanced process technology development is extremely challenging due to some anti-globalization, China technology roadmap has to be refocused to *More than Moore* path.
- *More than Moore* is one of the most promising technology, such as new structure, advanced package, specialized process technology
- China IC market capacity is huge in the post-Moore era for matured process technology nodes, due to diversified IC products on China market
- Education for Chip students would be engineering oriented instead of pure theoretic subject
- Globalization is the best way to develope IC technology. There would be NO WINNER if anti-globalization becomes reality
- Localized industry supply chain needs to be enhanced to secure IC industry in China, especially in epidemic peroid

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Thank You!

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ZJU-Hangzhou Global Scientific and Technological Innovation Center

Https：http://hic.zju.edu.cn/